

CHELSEA DJ2 UMA Schematics Document

AMD Danube CPU S1G4


RS880M + SB820M

2010-04-13

REV : X01

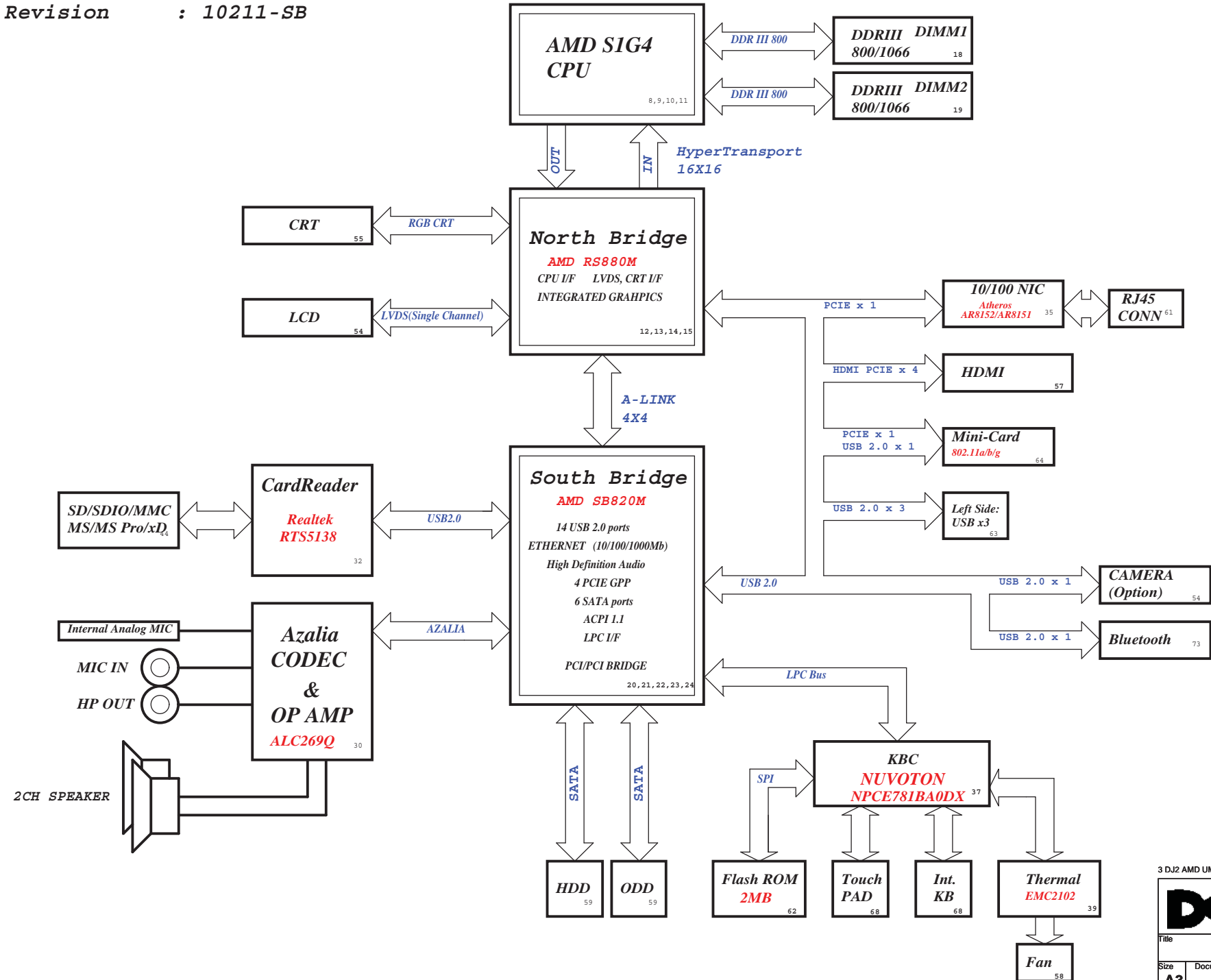
DY : Nopop Component
HDMI : Pop for HDMI function
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cover Page			
Size Custom	Document Number Chelsea DJ2 AMD UMA		Rev X01
Date: Tuesday, April 13, 2010	Sheet 1	of	90

Project code : 91.4EM01.001
PCB P/N : 48.4EM18.0SA
Revision : 10211-SB

Chelsea DJ2 AMD UMA Block Diagram



CHARGER	
BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC
SYSTEM DC/DC	
RT8205BGQW-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW
SYSTEM DC/DC	
RT8209EGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN
CPU CORE	
ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB
DDR III SUS&VTT	
TPS51116RGER 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS
SYSTEM DC/DC	
APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
Switches/RT9013 42,53	
INPUTS	OUTPUTS
+3.3V_ALW +5V_ALW +1.5V_SUS +3.3V_RUN	+3.3V_RUN +5V_RUN +1.5V_RUN +2.5V_RUN
SYSTEM DC/DC	
TPS51125RGER 48,51	
INPUTS	OUTPUTS
+3.3V_ALW +1.5V_SUS	+1.1V_ALW +CPU_VDDR
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Bottom	

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title		
Block Diagram		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
Date:	Sheet	of
Tuesday, April 13, 2010	2	90

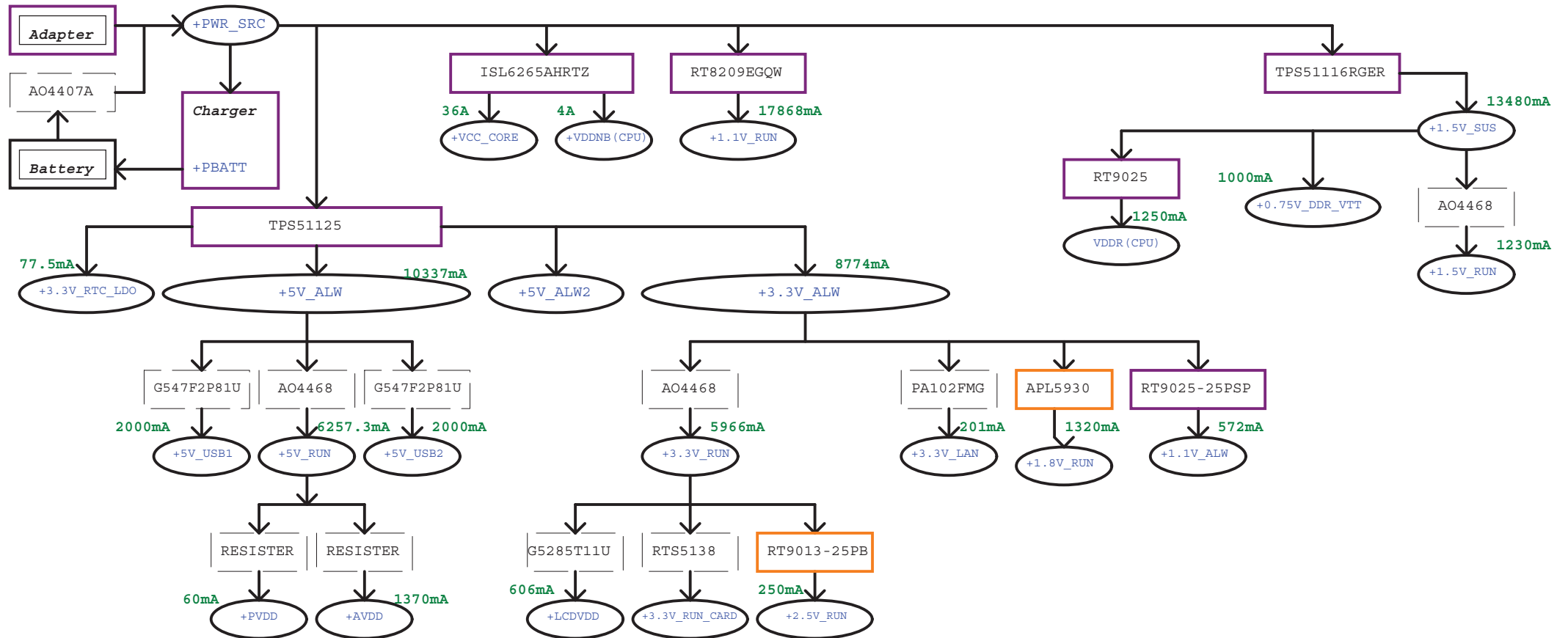
Power Block Diagram

Power Shape

Regulator

LDO

Switch



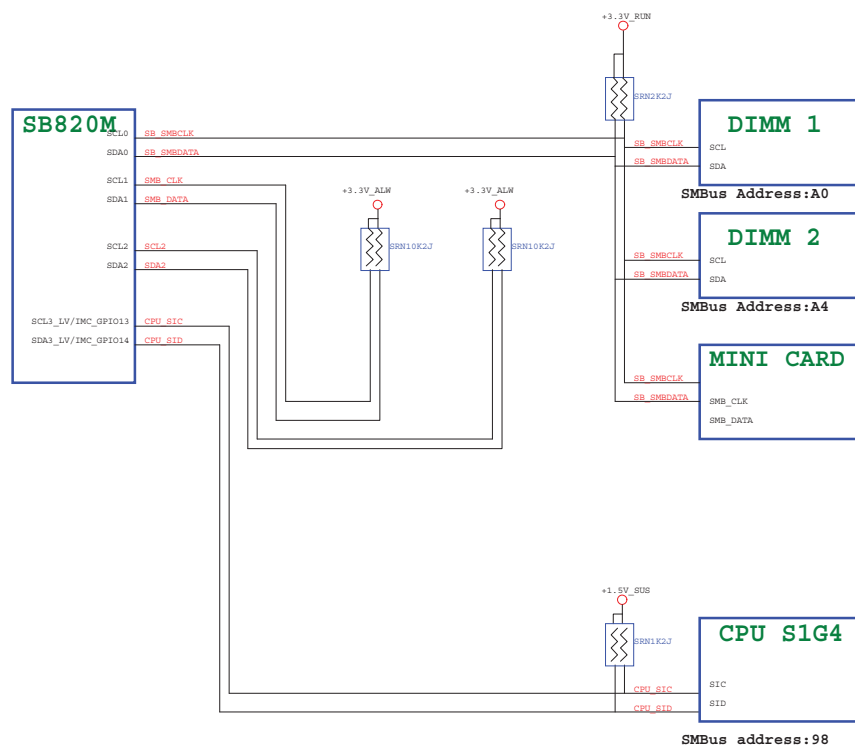
3 DJ2 AMD UMA (10 100 w HDMI)



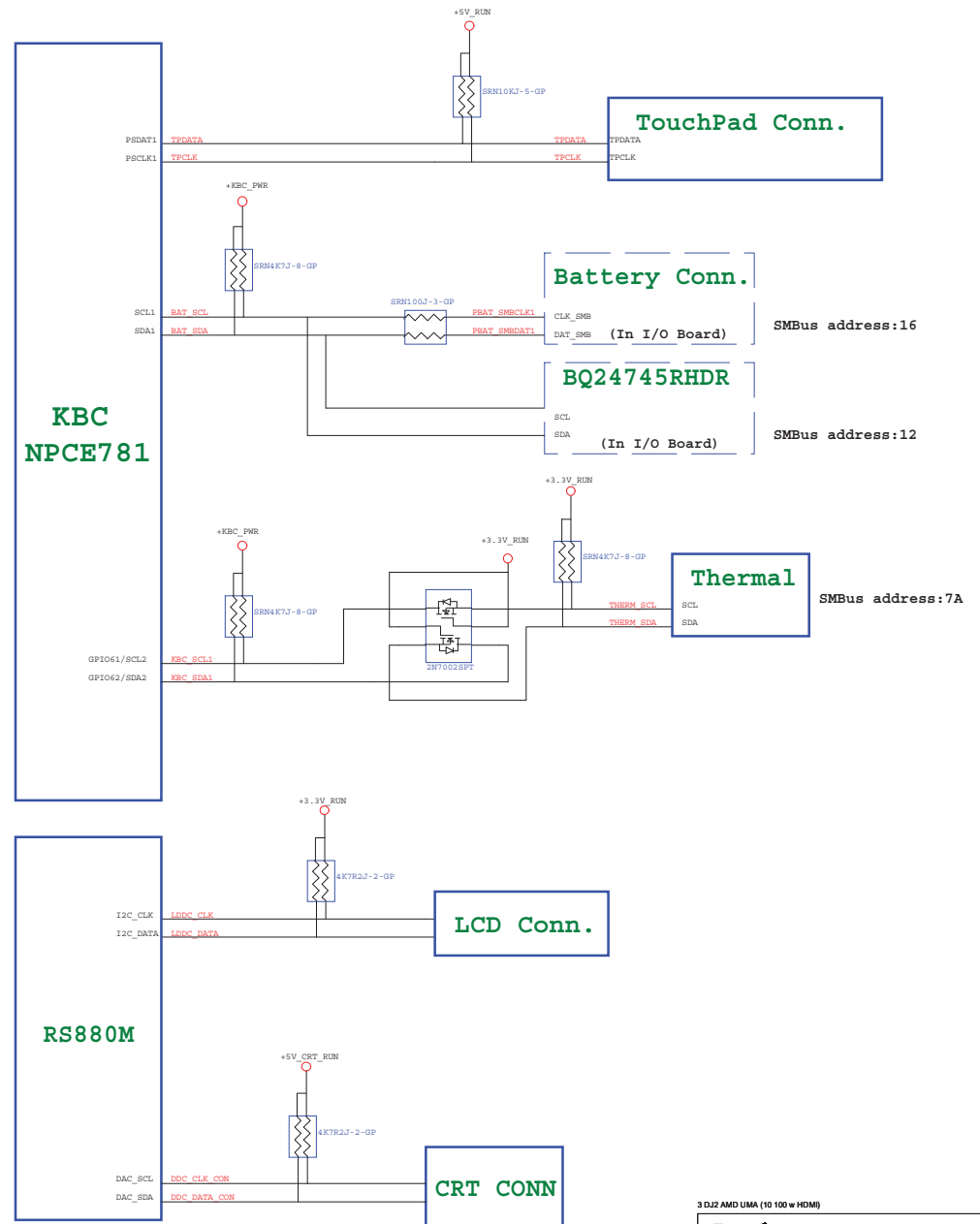
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Power Block Diagram	
Size	Document Number	Rev		
Custom	Chelsea DJ2 AMD UMA	X01		
Date:	Tuesday, April 13, 2010	Sheet	3	of 90

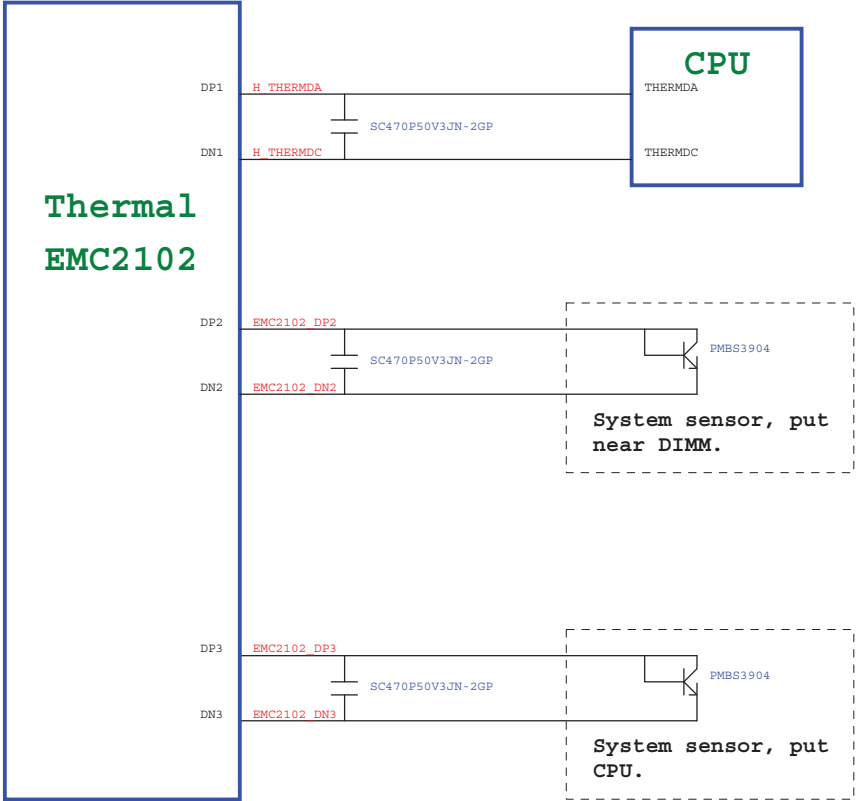
SB820M SMBus Block Diagram



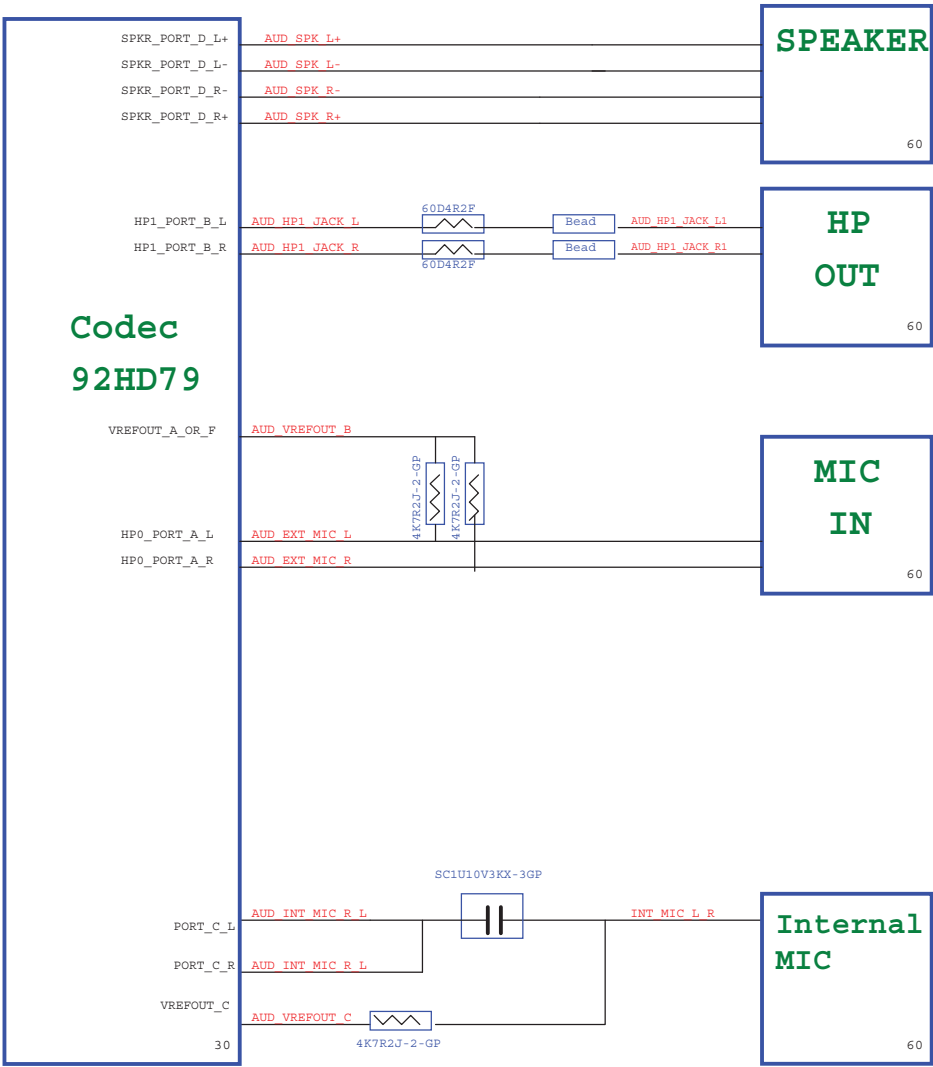
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 ROMTYPE_0 ROM TYPE 3.3V 0V SPI ROM 3.3V 3.3V Reserved 0V 0V Firmware Hub 0V 3.3V LPC ROM * (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2 COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interface is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V- Reserved. * 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113 rs880m ds nda 1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table


USB	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB1 (I/O Board, 17")
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	Reserve
10	CARD READER
11	CAMERA
12	BLUETOOTH
13	Reserve

PCIe Routing

LANE0	MiniCard WLAN
LANE1	LAN

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Clock Generator ICS9LPRS480

Size

Custom

Document Number

Chelsea DJ2 AMD UMA

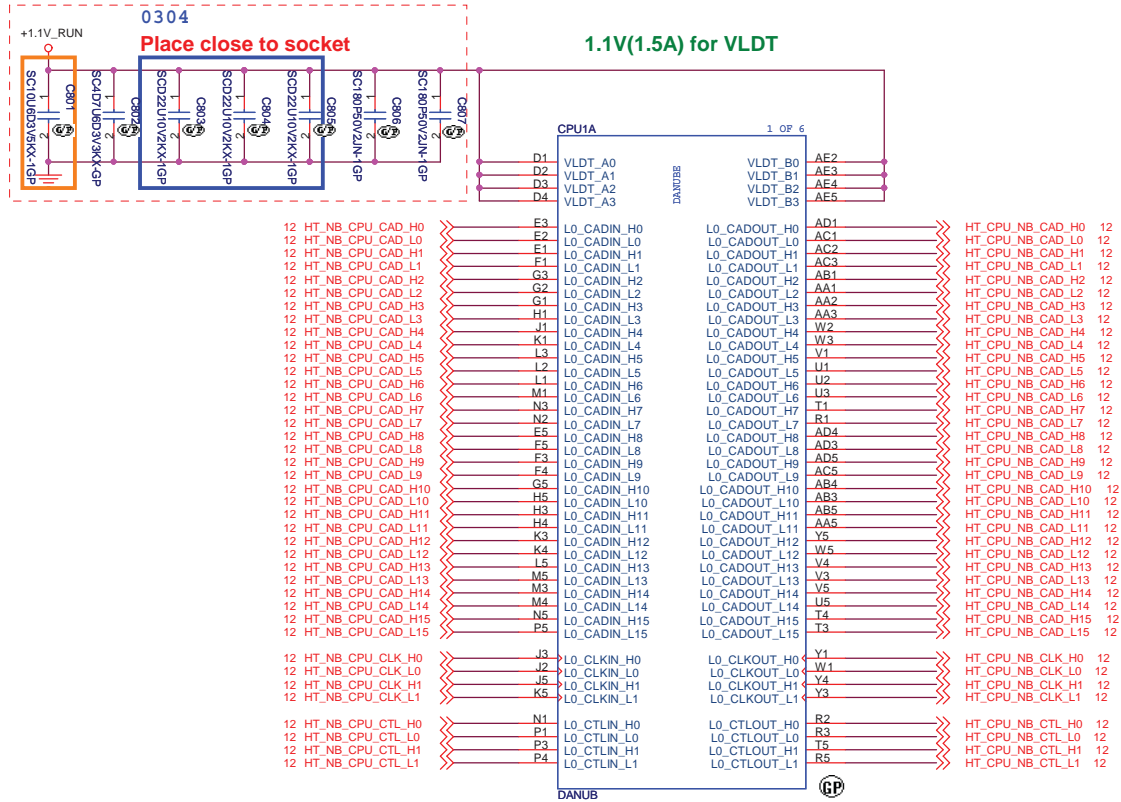
Rev

X01

Date: Tuesday, April 13, 2010

Sheet 7 of 90

SSID = CPU



SKT-BGA638H176

1'nd 62.10055.111

2'nd 62.10055.181

3 DJ2 AMD UMA (10 100 w HDMI)

SSID = CPU

4.70UF*4
0.22UF*4
1000PF*4
180PF*4

Place near to CPU

0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V--DDR1333 (1.75A)

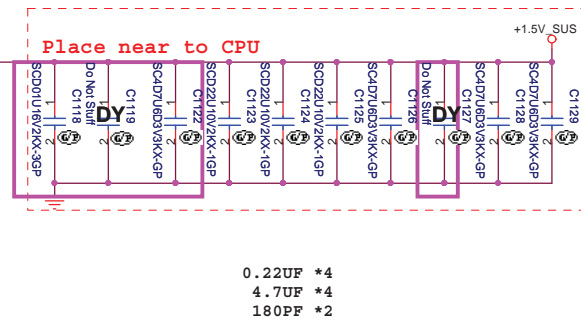
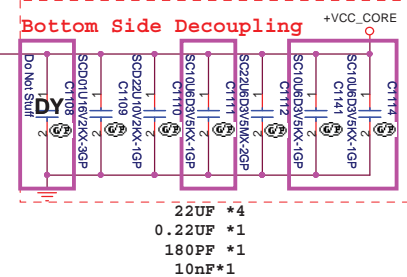
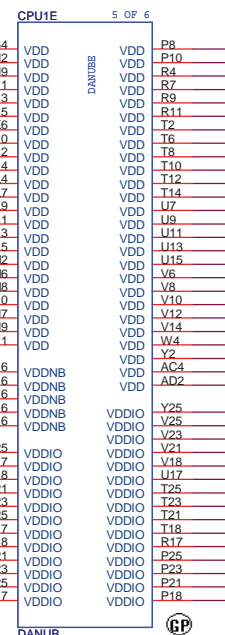
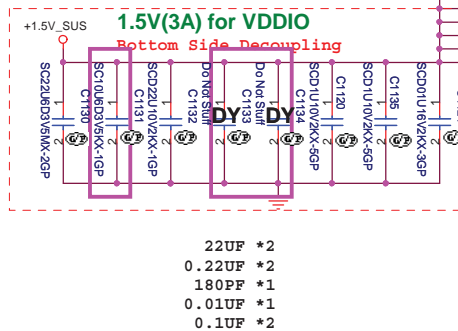
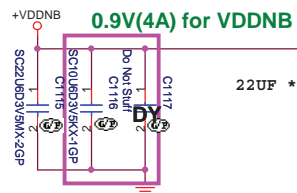
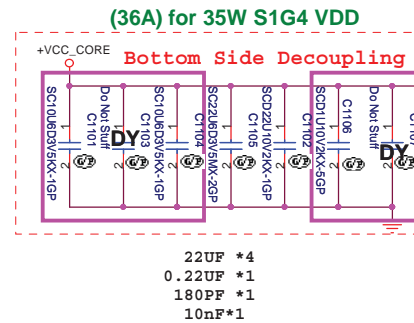
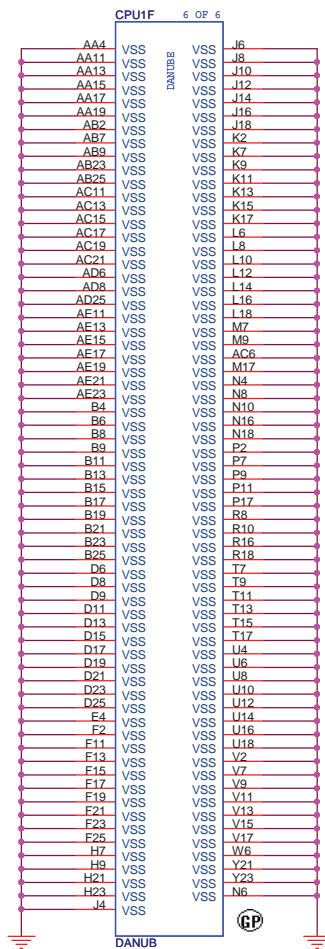
CLOSE TO CPU

DANUB
3 D12 AMD UMA (10 100 w HDMI)



Title CPU DDR(2/4)		
Size Custom	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 9	of 90

SSID = CPU



3 DJ2 AMD UMA (10 100 w HDMI)

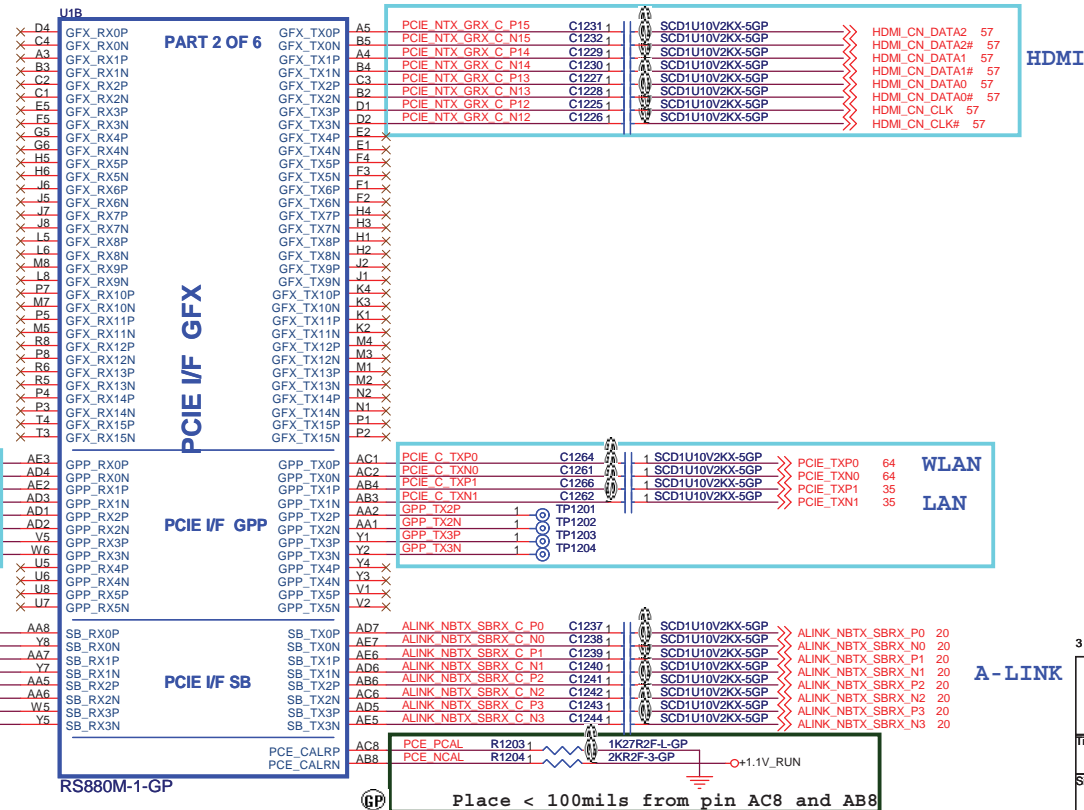
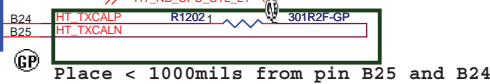
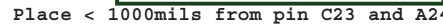


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CPU_Power_(4/4)

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
Date: Tuesday, April 13, 2010	Sheet 11 of 90	

RS880M : 71.RS880.M05



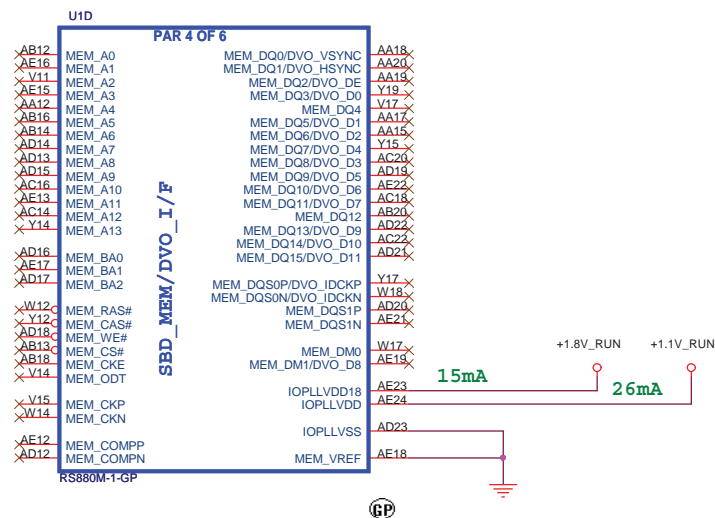
3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title AMD-RS880M_HT LINK&PCIe(1/4)			
Size Custom	Document Number Chelsea DJ2 AMD UMA		Rev X01
Date: Tuesday, April 13, 2010	Sheet 12	of 90	

SSID = N.B



3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title
AMD-RS880M_SidePort_(3/4)

Size A3 Document Number **Chelsea DJ2 AMD UMA** Rev **X01**

Date: Tuesday, April 13, 2010 Sheet 14 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

Date: Tuesday, April 13, 2010	Sheet 16 of 90
-------------------------------	----------------

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA

Rev
X01

Date: Tuesday, April 13, 2010

Sheet 17 of 90

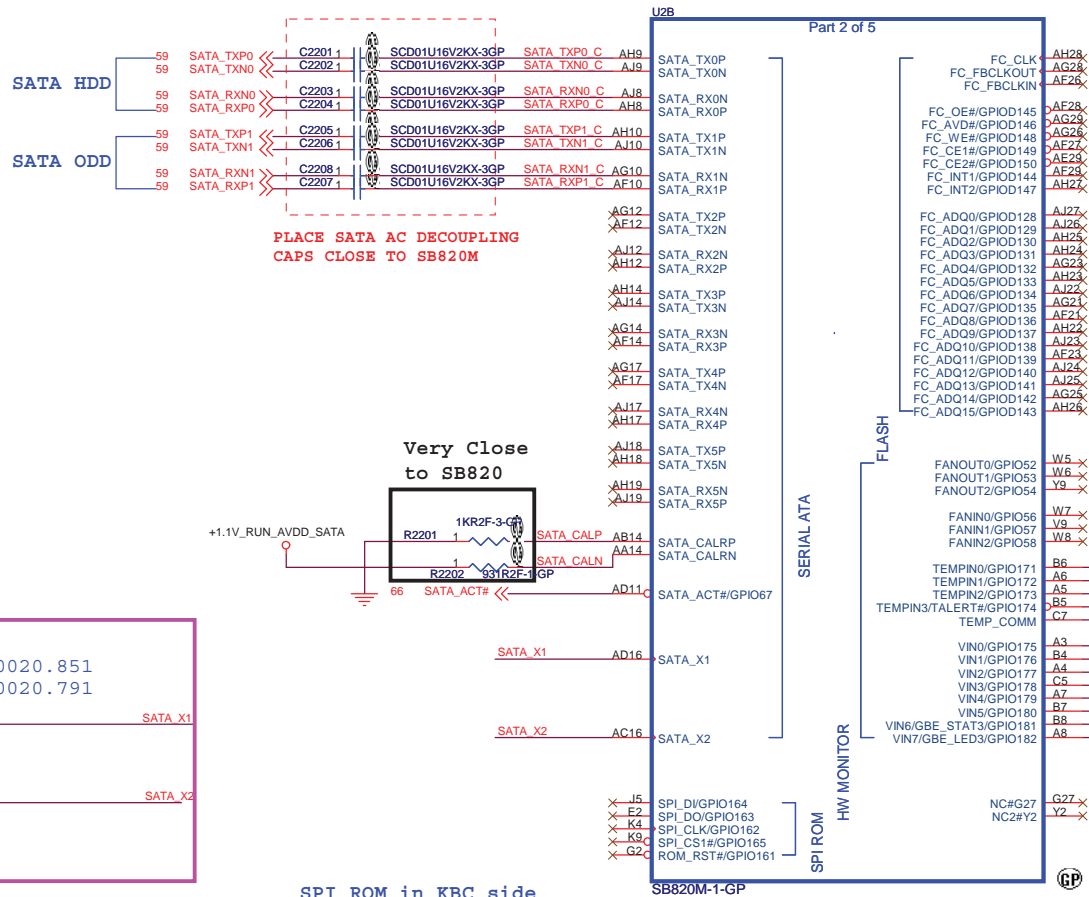
SB700 A12 : 71.SB800.M02



Size A3	Document Number Chelsea D 12 AMD LIMA	Rev y
------------	---	----------

Date: Tuesday, April 13, 2010 Sheet 20 of 90

SSID = S.B

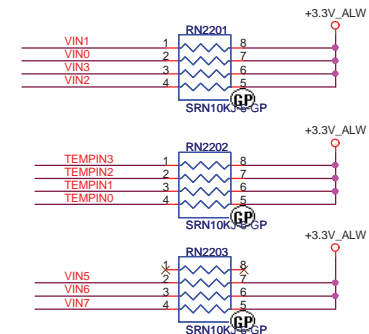


GPIO[150:128] are open drain GPIO pins where as GPO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

If use as GPIO, need to pull up to 1.8V_RUN

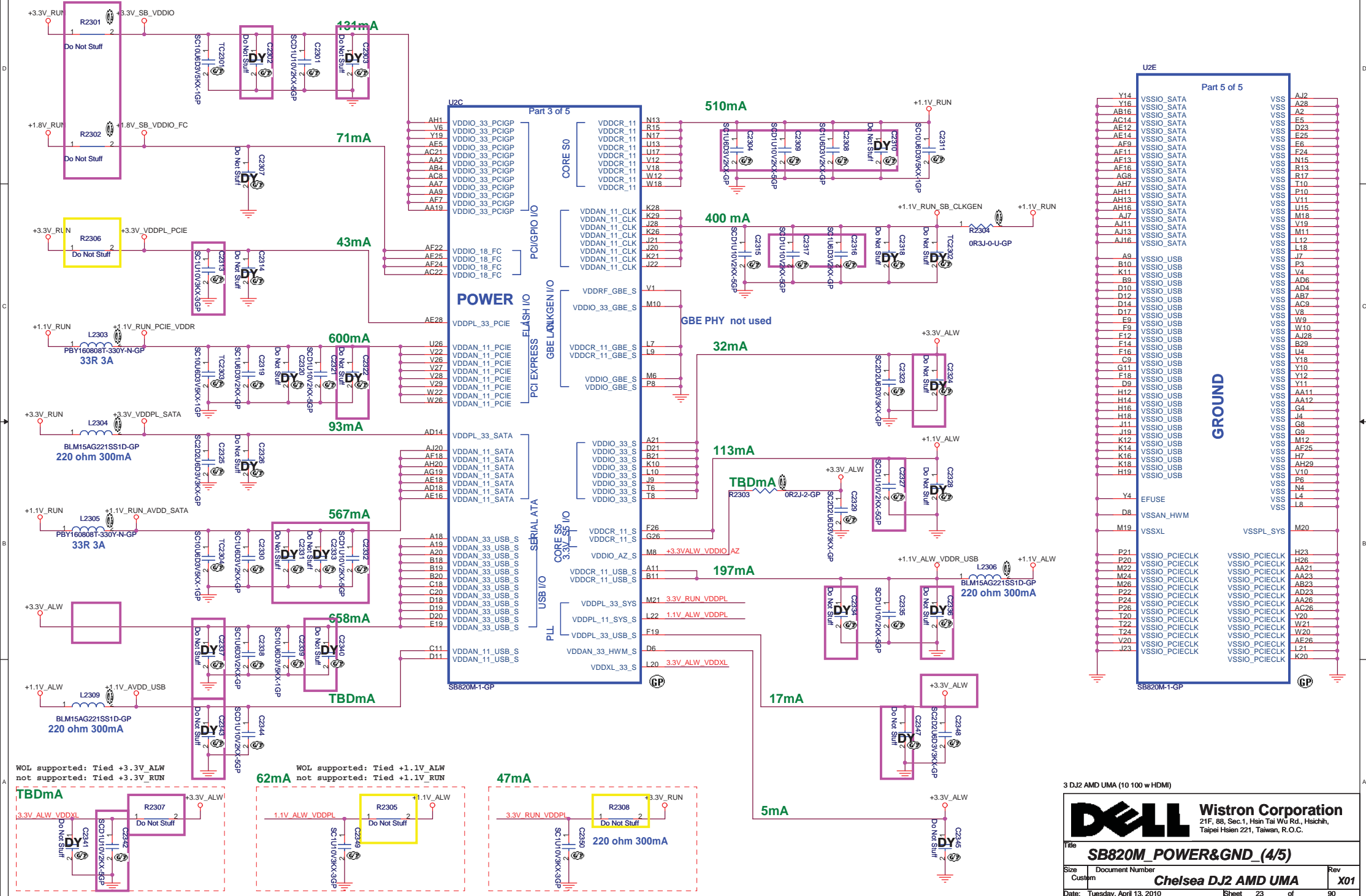
suggest not use HW monitor

MEM_1V5 51



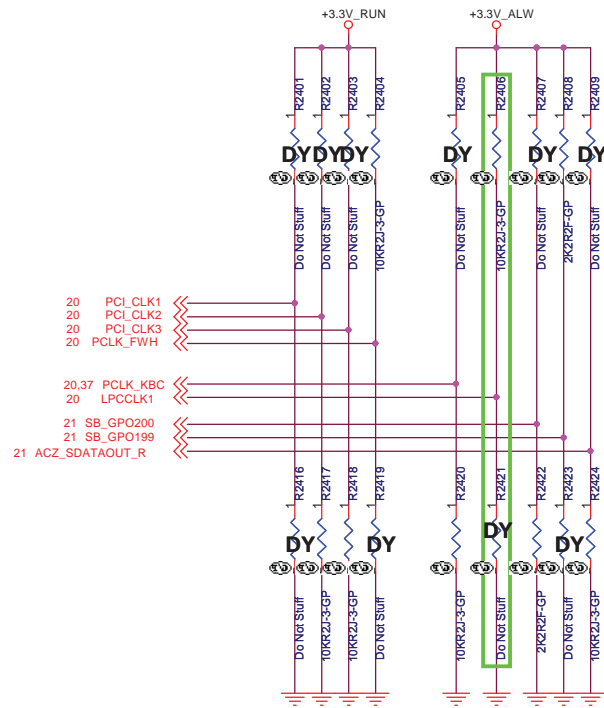
3 DJ2 AMD UMA (10-100 w HDMI)

SSID = S.B

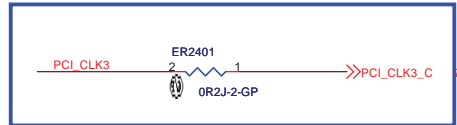


SSID = S.B

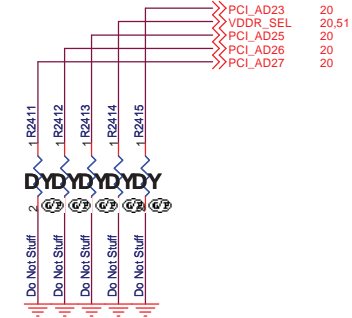
REQUIRED STRAPS



0309



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

3 DJ2 AMD UMA (10 100 w HDMI)

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VCC CORE)

Size

Document Number

Rev

Chelsea DJ2 AMD UMA**X01**

Date: Tuesday, April 13, 2010

Sheet 25 of 90

1

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VCC GFXCORE)

Size

Document Number

Rev

Chelsea DJ2 AMD UMA

X01


Date: Tuesday, April 13, 2010

Sheet 26 of 90

1

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

Document Number

Rev

Chelsea DJ2 AMD UMA


X01

Date: Tuesday, April 13, 2010

Sheet 27 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Date: Tuesday, April 13, 2010

Rev
X01

Sheet 28 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

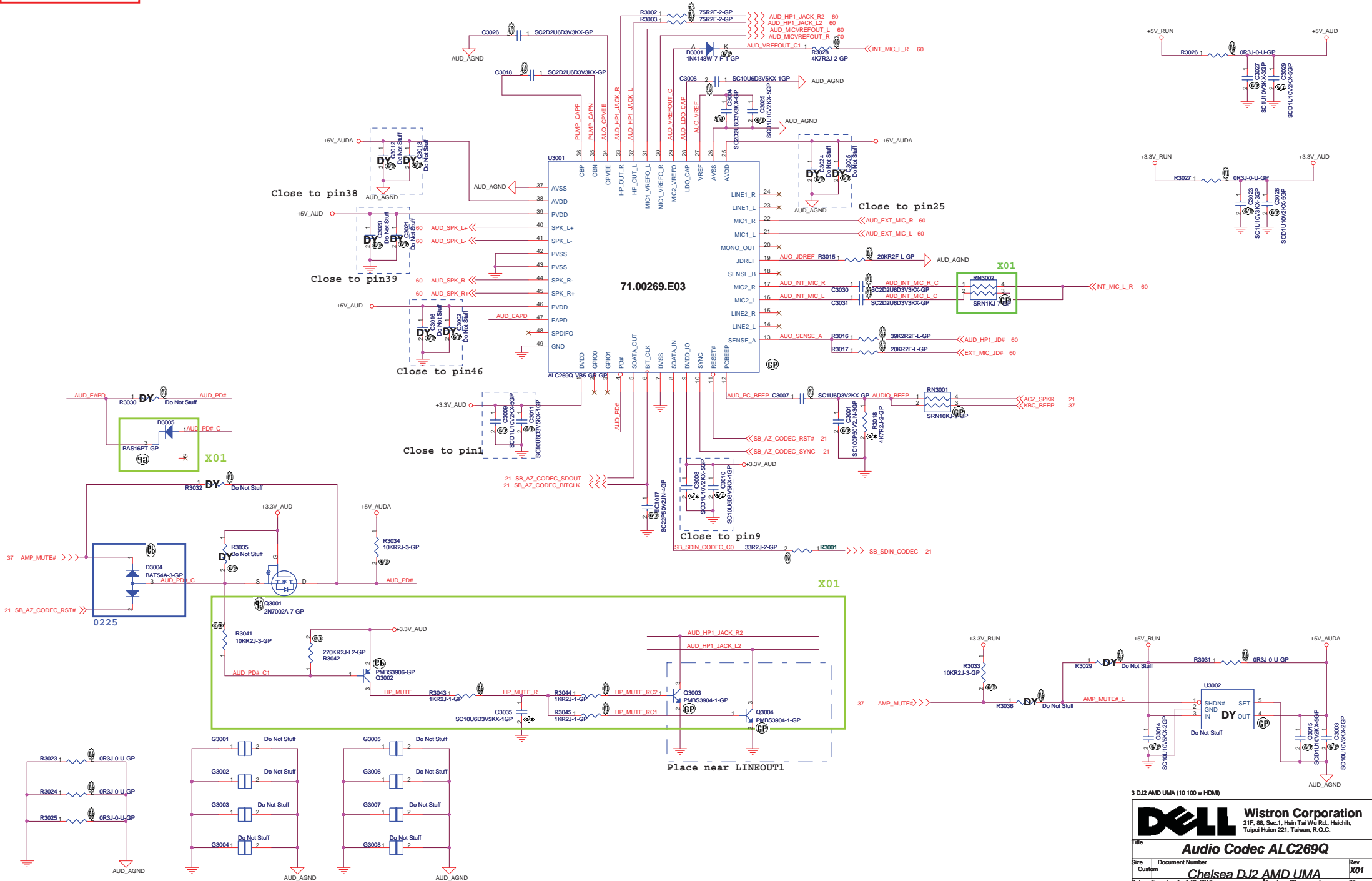
Document Number
Chelsea DJ2 AMD UMA

Date: Tuesday, April 13, 2010

Rev
X01

Sheet 29 of 90

SSID = AUDIO



3 DJ2 AMD UMA (10 100 w HDMI)




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				Audio Codec ALC269Q			
Size	Custom	Document Number				Rev	X01
		Chelsea D/I2 AMD UMA					
Date: Tuesday, April 13, 2010				Sheet	30	of	90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

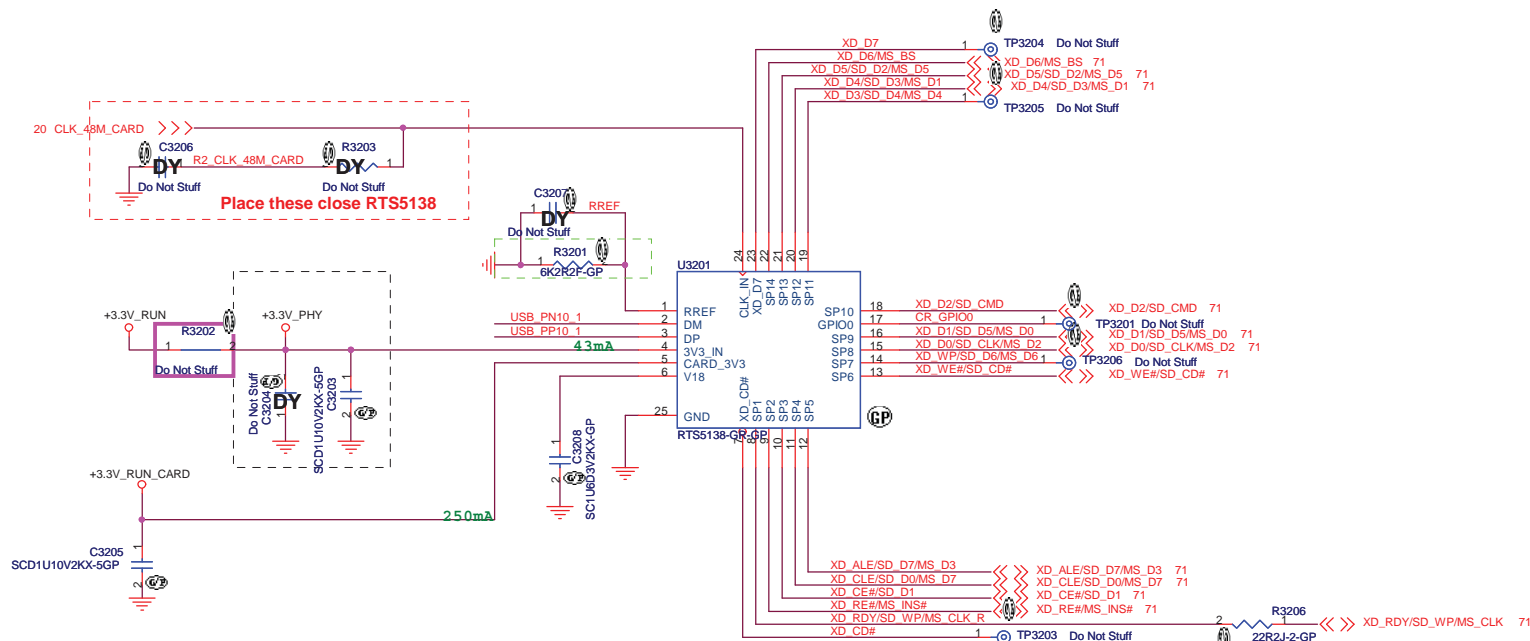
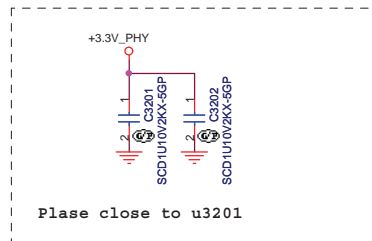
Document Number
Chelsea DJ2 AMD UMA

Rev
X01

Date: Tuesday, April 13, 2010

Sheet 31 of 90

SSID = SDIO




3 DJ2 AMD UMA (10 100 w HDMI)

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Card Reader-RTS5138					
Size	Document Number	Rev			
Custom	Chelsea DJ2 AMD UMA				X01
Date:	Tuesday, April 13, 2010	Sheet	32	of	90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

Date: Tuesday, April 13, 2010	Sheet 33 of 90
-------------------------------	----------------

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

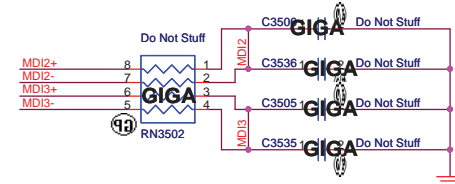
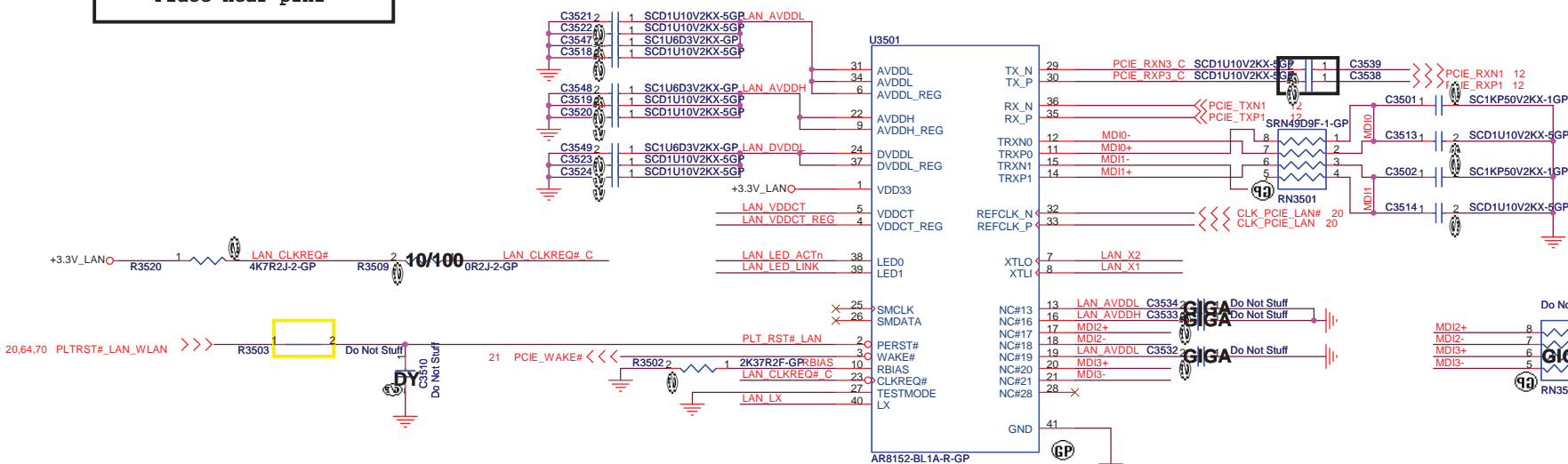
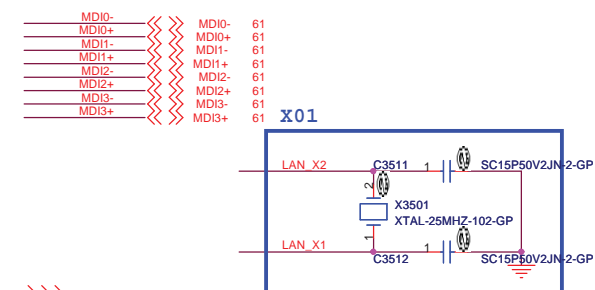
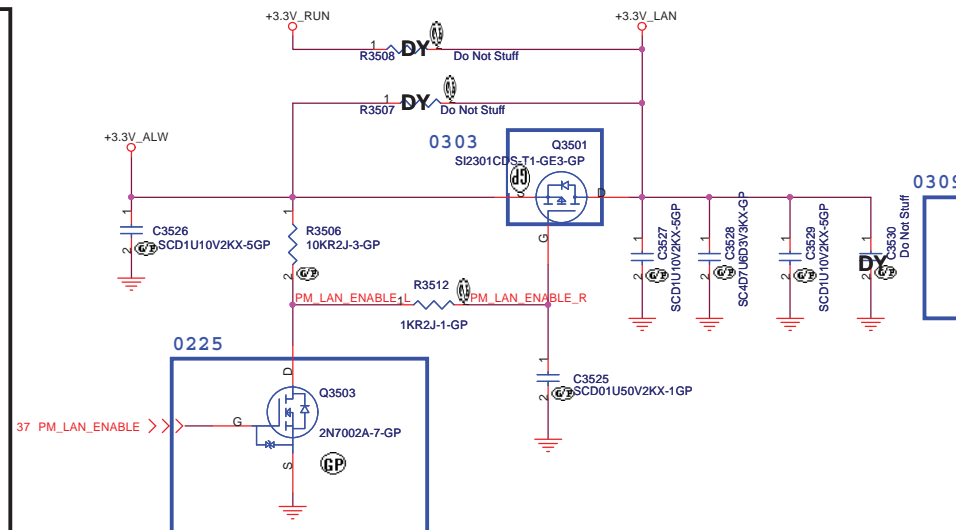
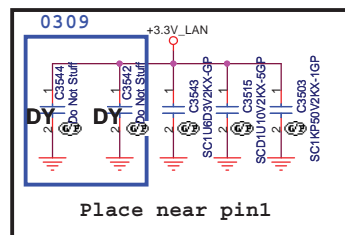
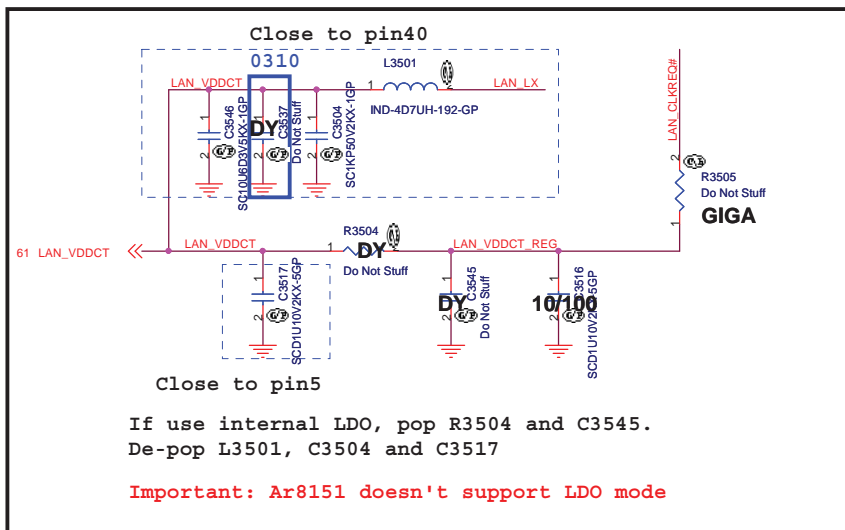
Size
A3

Document Number
Chelsea DJ2 AMD UMA

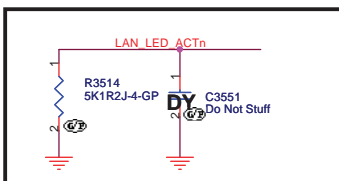
Date: Tuesday, April 13, 2010

Rev
X01

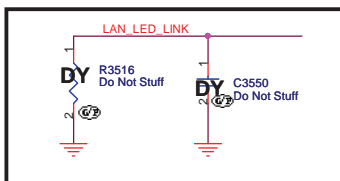
Sheet 34 of 90



If overclocking, de-pop R3514
and C3551




If use LDO mode, pop R3516
and C3550



GIGA LAN use 71.08151.003

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Rev
X01

Date: Tuesday, April 13, 2010

Sheet 36 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Rev
X01

Date: Tuesday, April 13, 2010

Sheet 38 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

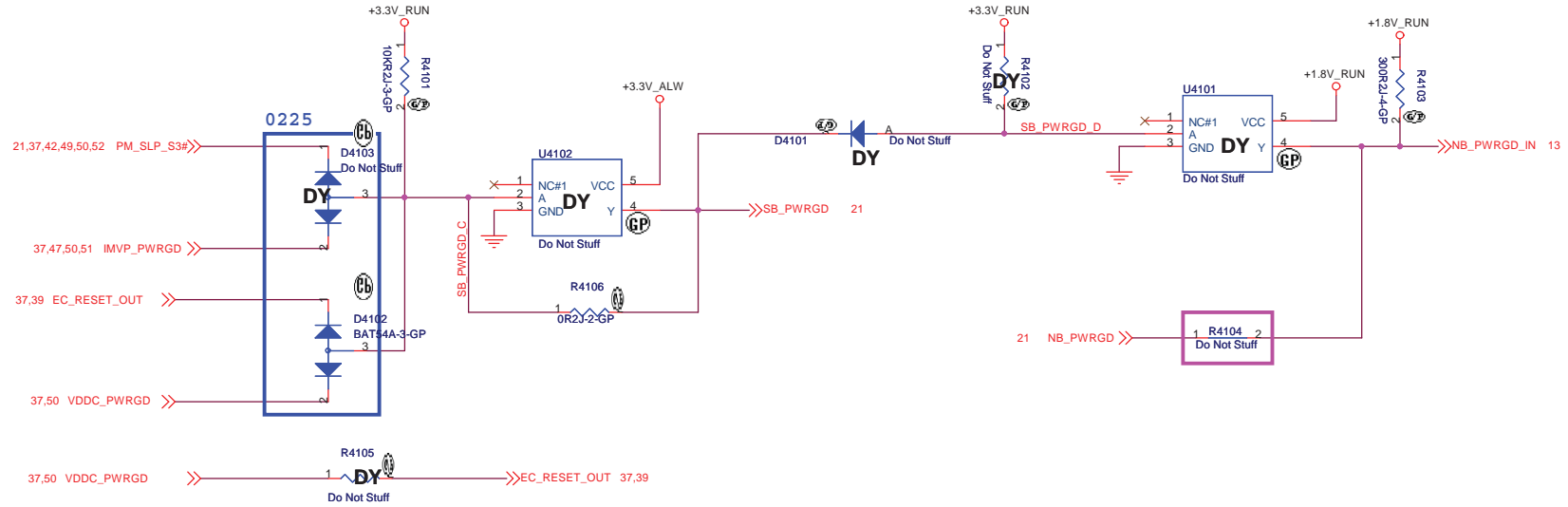
Title

Reserved

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

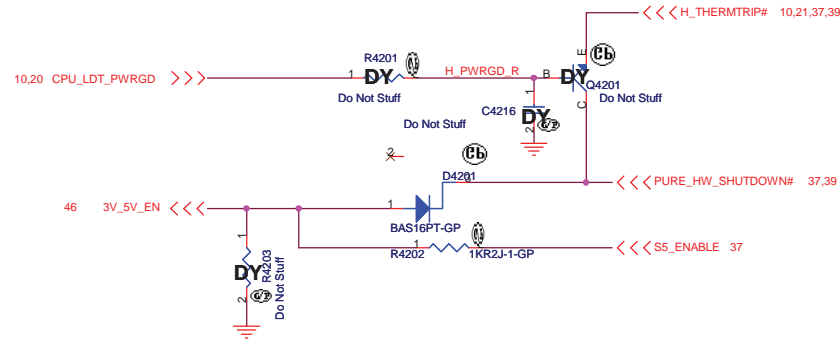
Date: Tuesday, April 13, 2010	Sheet 40 of 90
-------------------------------	----------------

SSID = Reset.Suspend

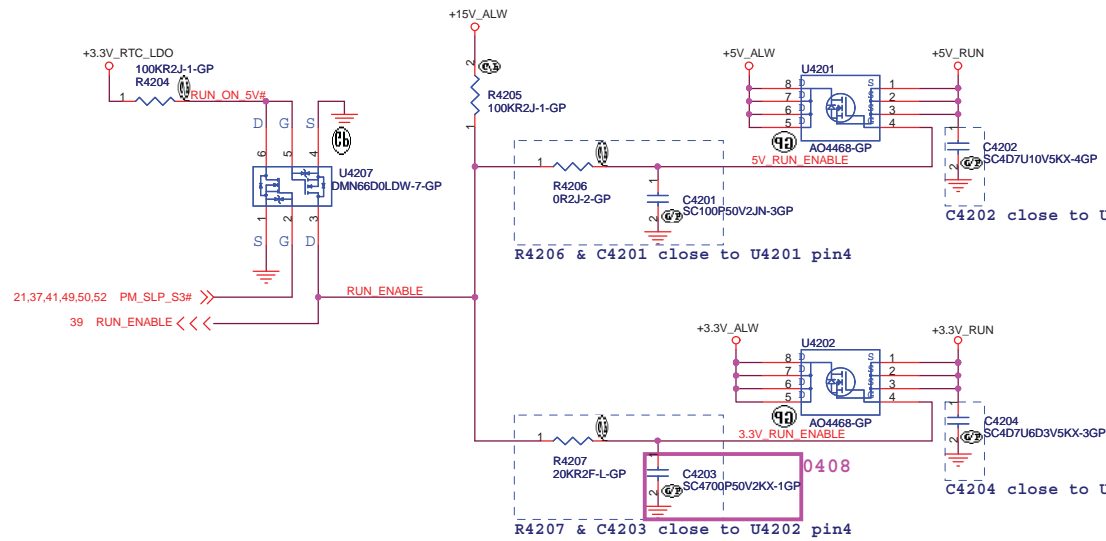


3 DJ2 AMD UMA (10 100 w HDMI)

SSID = Reset.Suspend

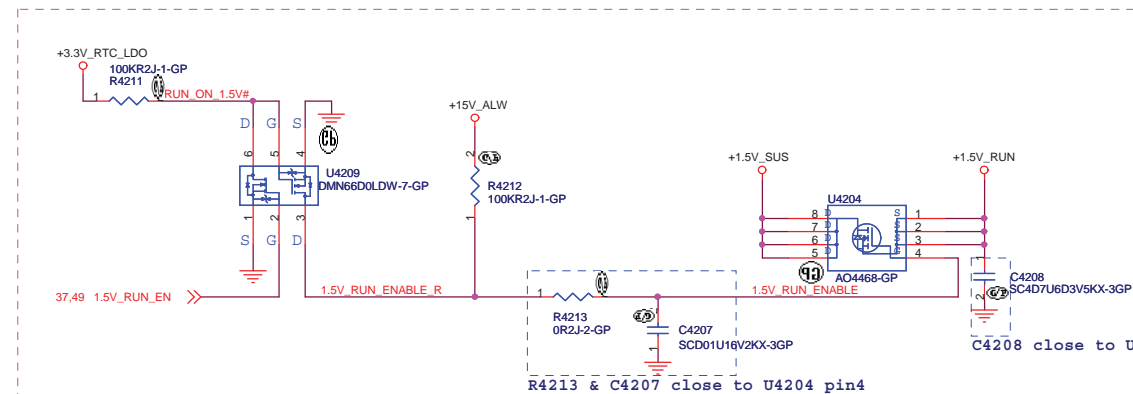


Run Power

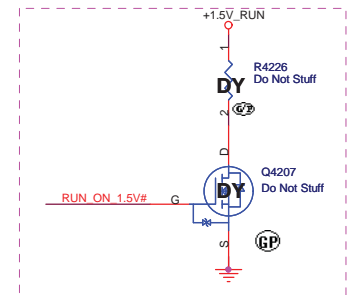


Peak current: 6257.3mA (HD:1100 ODD:2500)
 Design current: 4380.11 mA
 11.6A
 Rds=14m ohm

Peak current: 5966mA
 Design current: 4177 mA
 11.6A
 Rds=14m ohm



Peak current: 1230mA
 Design current: 861 mA
 11.6A
 Rds=14m ohm



3 DJ2 AMD UMA (10 100 w HDMI)

DCIN CONN



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Date	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

DCIN

Size
A3

Document Number

Chelsea DJ2 AMD UMA

Rev
X01

Date: Tuesday, April 13, 2010

Sheet 43 of

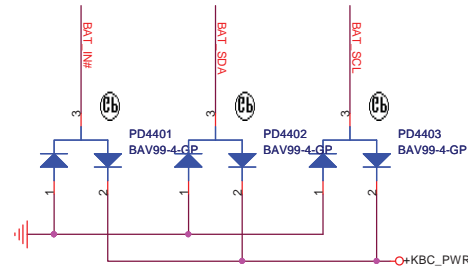
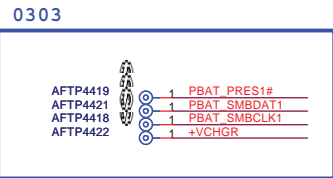
Sheet	43	of	90
-------	----	----	----

BATT1

20.80864.009

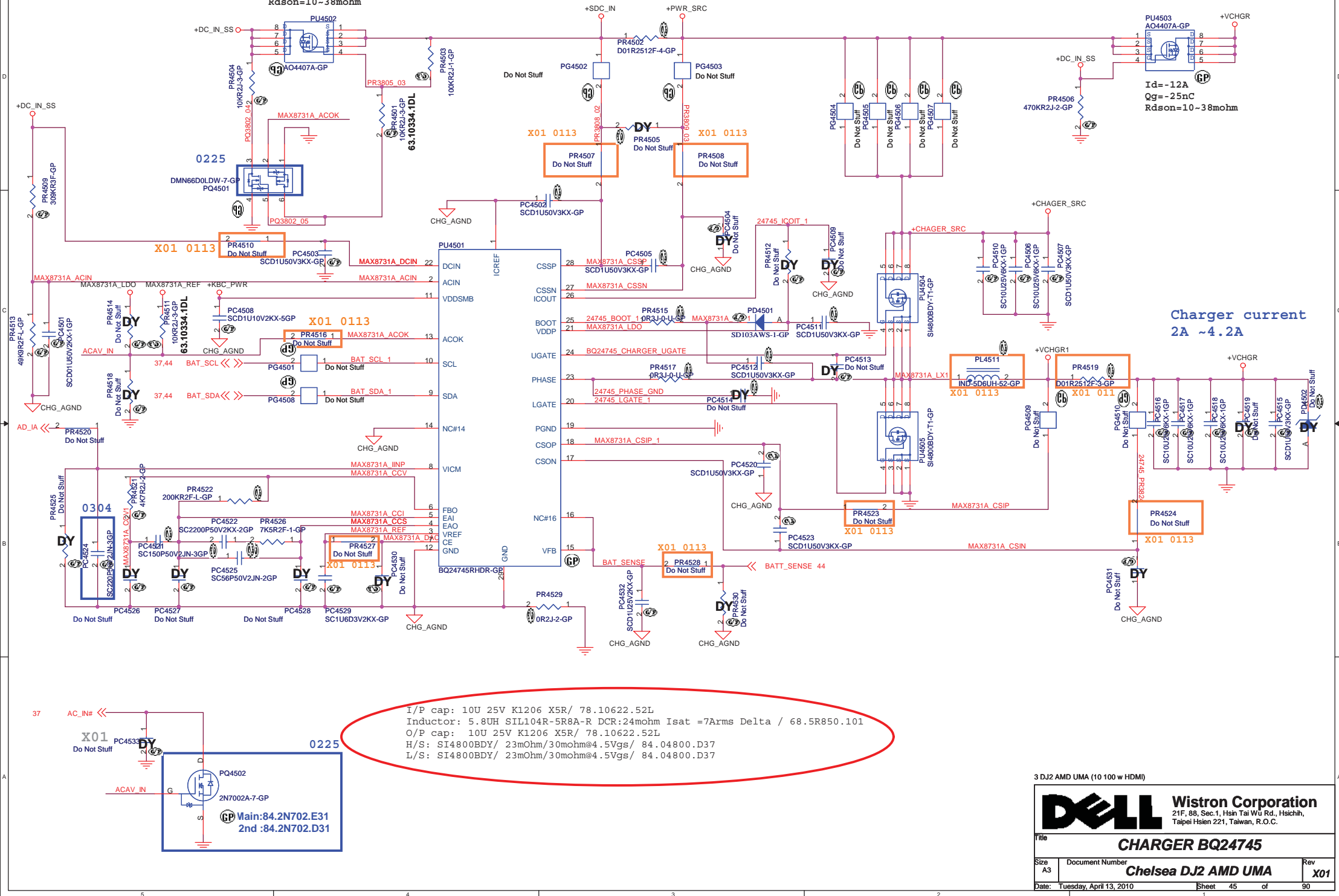
SYN-CON9-4-GP-U

Pin 11 is connected to GND.



SSID = Charger

Id=-12A
Qg=-25nC
Rdson=10~38mohm



3 DJ2 AMD UMA (10 100 w HDMI)

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CHARGER BQ24745			
Size A3	Document Number	Rev X01	
Chelsea DJ2 AMD UMA			
Date: Tuesday, April 13, 2010	Sheet 45	of 90	

Design Current = 7.57A
11.89A < OCP < 14.053A

Design Current = 7.3A
11.45A < OCP < 16A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.537

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.537

RT8205B(T4.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VRBG3	300kHz	375kHz
VRBG5	365kHz	460kHz

RT8205B(T4.08208.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VRBG3	365kHz	460kHz
VRBG5	365kHz	460kHz

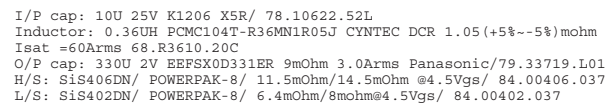
TPSS1125	74.51125.073
RT8205BQGW	74.08205.B73

SKIPSEL	VREG3 or VRBG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

3 DJ2 AMD UMA (10 100 w HDMI)

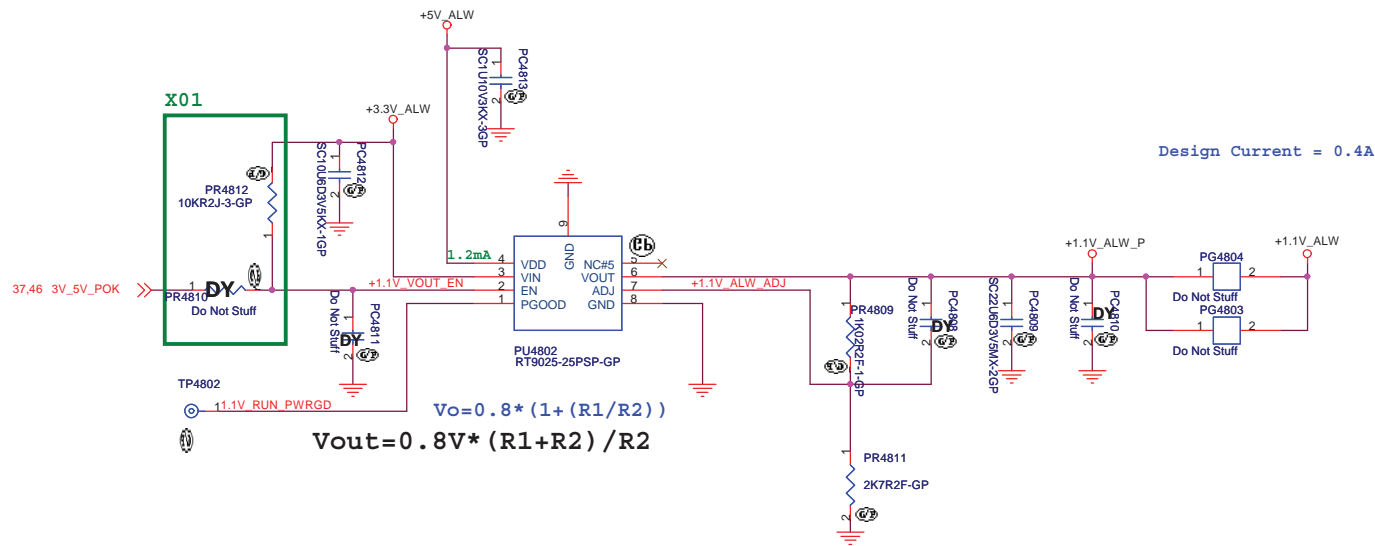
ISL6265HRTZ-T for +VCC_CORE&+VDDNB



Title			
VREG : +VCC_CORE&+VDDNB			
Size	Document Number	Rev	
A2	Chelsea DJ2 AMD UMA	X01	
Date:	Tuesday, April 13, 2010	Sheet 47 of	90

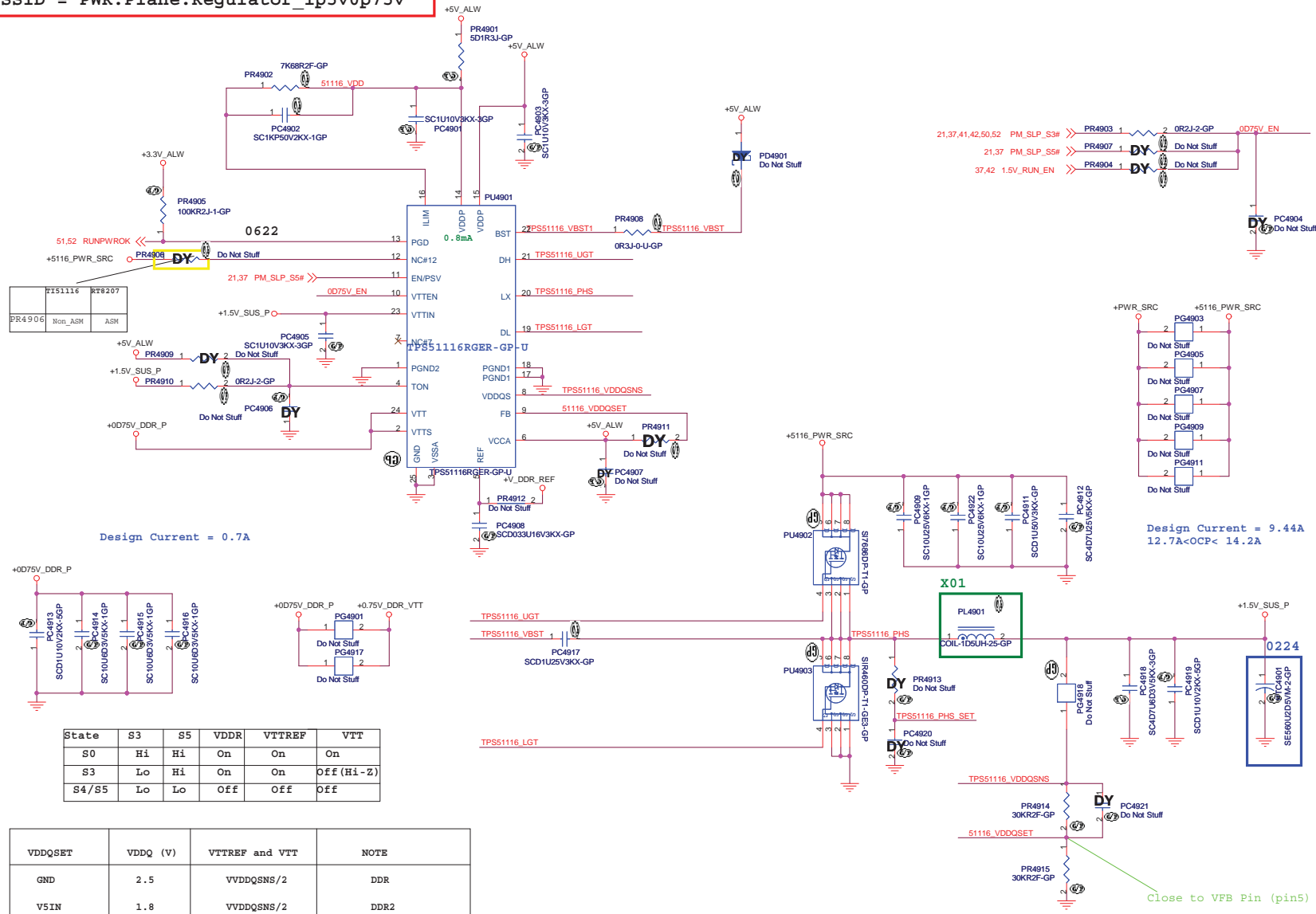
SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW



3 DJ2 AMD UMA (10 100 w HDMI)

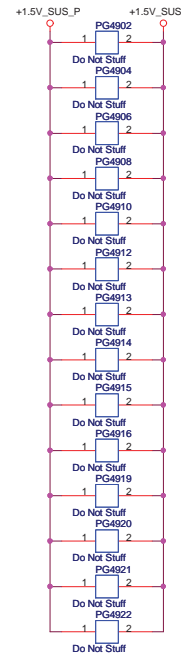
SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFXC0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37



3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5116RGER +1.5V SUS**

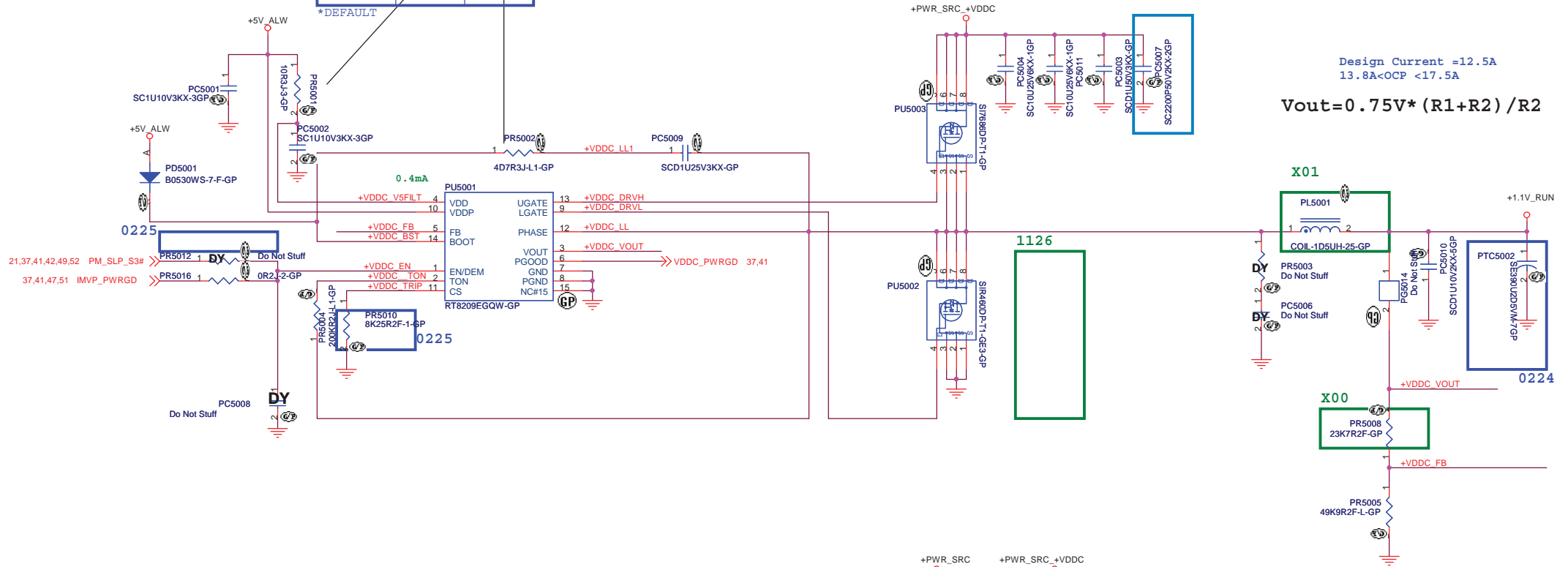
Size: Custom Document Number: **Chelsea DJ2 AMD UMA** Rev: **X01**

Date: Tuesday, April 13, 2010 Sheet: 49 of 90

SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT

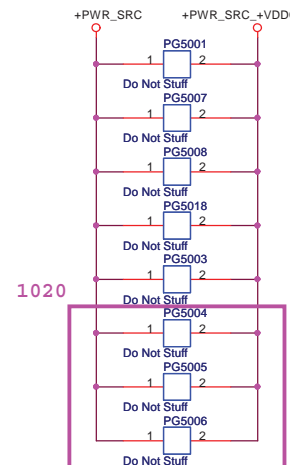


Design Current =12.5A
13.8A<OCP <17.5A

$$V_{out} = 0.75V * (R1 + R2) / R2$$

21,37,41,42,49,52 PM_SLP_S3# >> PR5012 1 DY Do Not Stuff
37,41,47,51 IMVP_PWRGD >> PR5016 1 0R2-2-GP

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037



3 DJ2 AMD UMA (10 100 w HDMI)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RT8209 +1.1V RUN

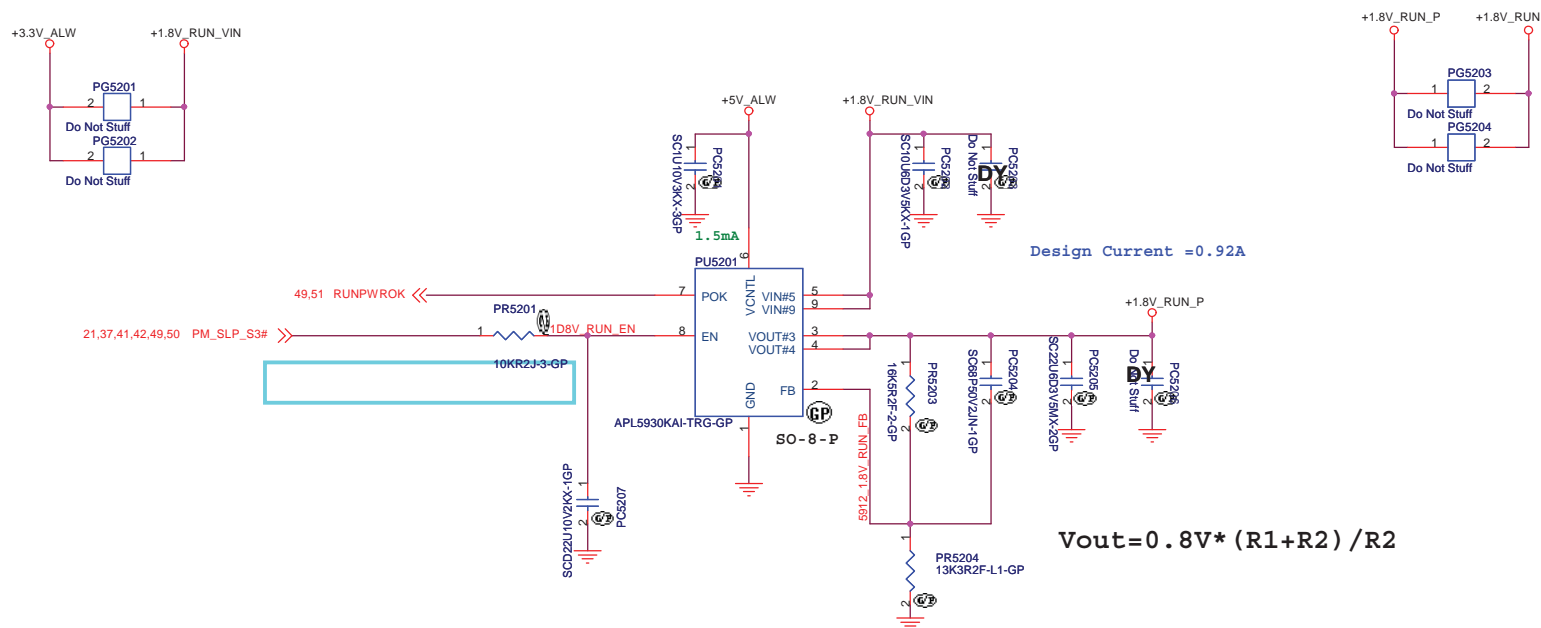
Size A3 Document Number
Chelsea DJ2 AMD UMA

Date: Tuesday, April 13, 2010 Sheet 50 of 90

Rev
X01


```
SSID = PWR.Plane.Regulator_1p8v
```

APL5930 for +1.8V_RUN



3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

APL5930 +1.8V RUN

Size
A3

Document Number

Chelsea DJ2 AMD UMA

Rev	X0
-----	-----------

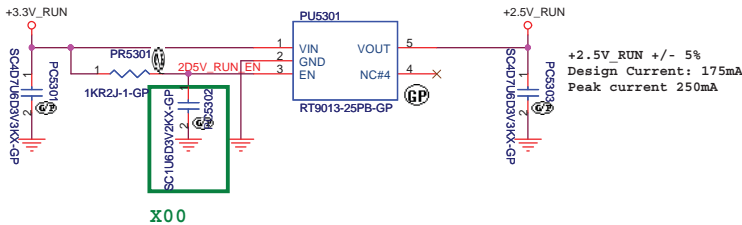
Date: Tuesday, April 13, 2010

Sheet 52 of

90

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN

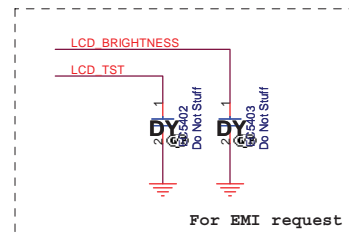
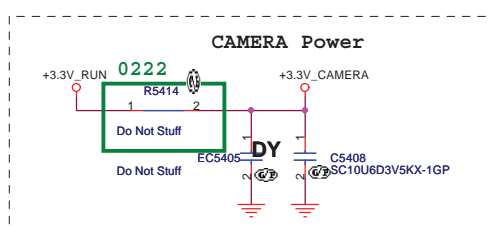
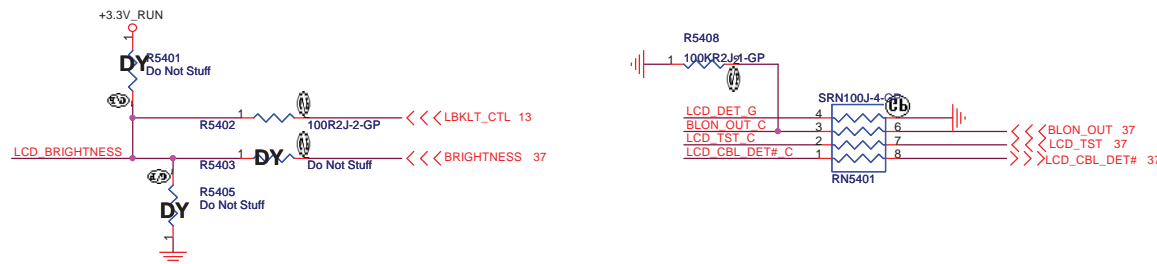
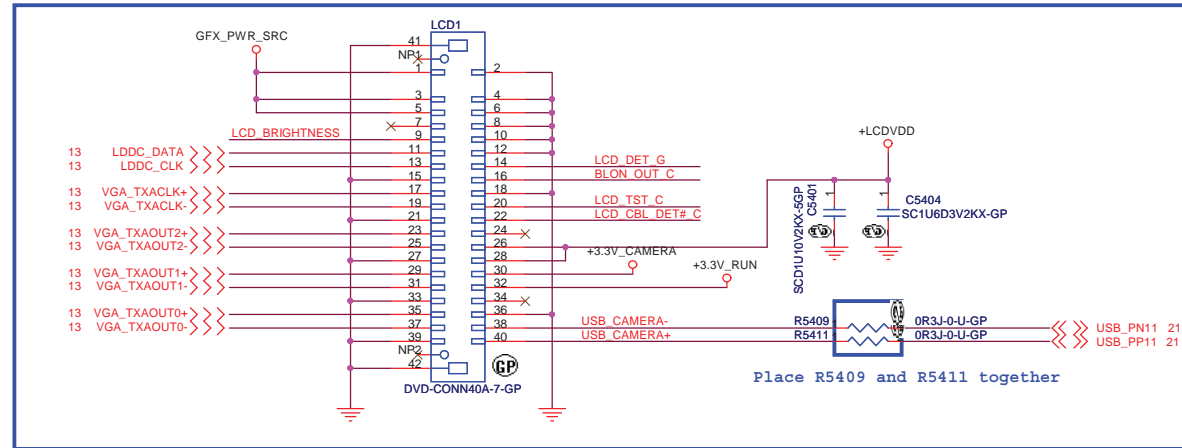


3 DJ2 AMD UMA (10 100 w HDMI)

SSID = VIDEO

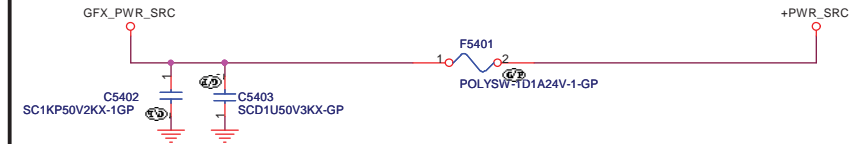
LVDS CONNECTOR

0225



SSID = Inverter

INVERTER POWER

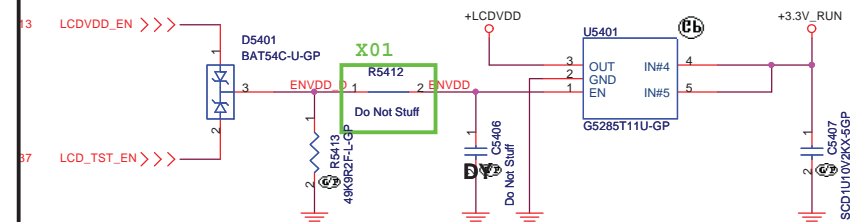


0224



SSID = VIDEO

LCD POWER



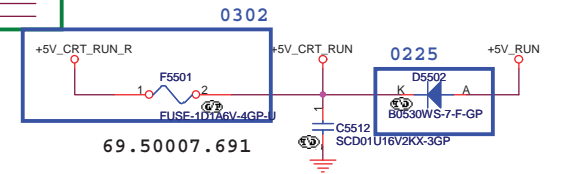
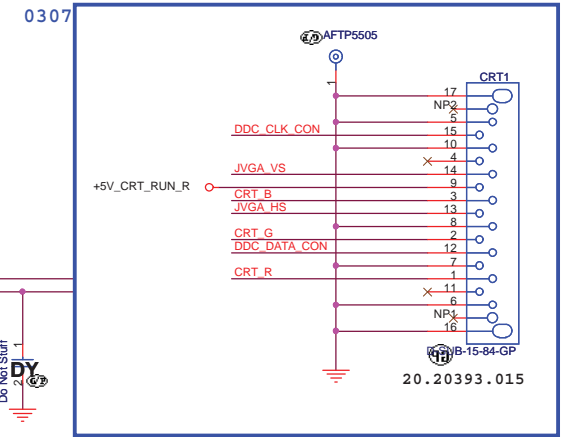
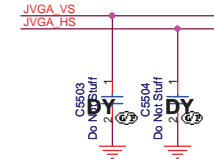
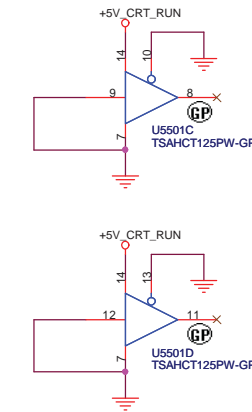
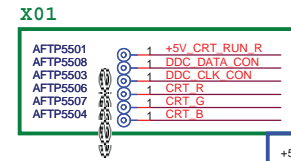
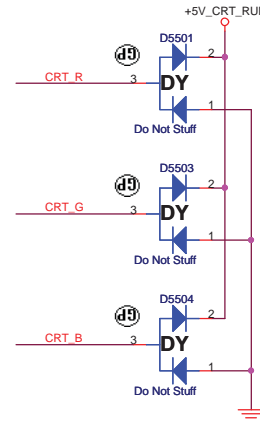
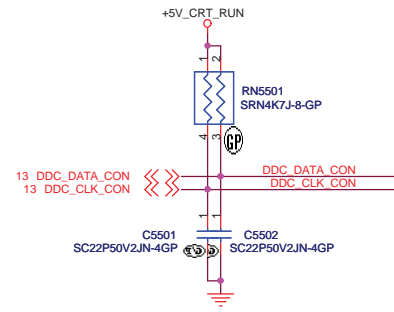
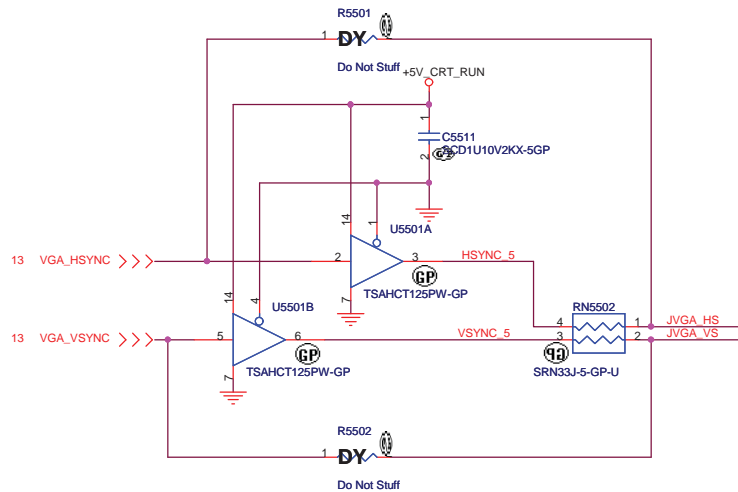
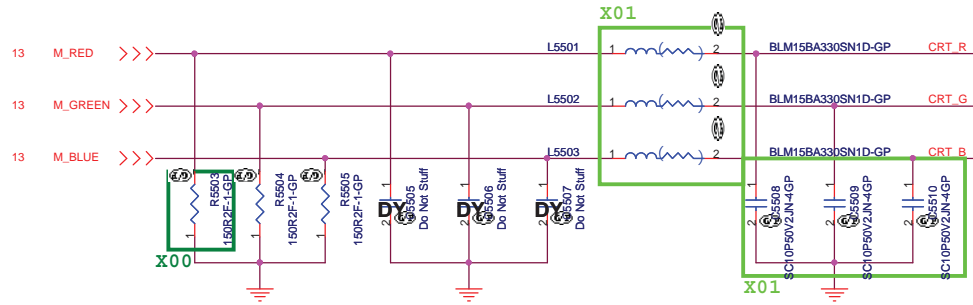
3 DJ2 AMD UMA (10 100 w HDMI)

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>LCD/Inverter Connector</i>			
Size A3	Document Number <i>Chelsea DJ2 AMD UMA</i>		Rev <i>X01</i>
Date:	Tuesday, April 13, 2010	Sheet 54 of	90

SSID = VIDEO

Layout Note:


- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



3 DJ2 AMD UMA (10 100 w HDMI)

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

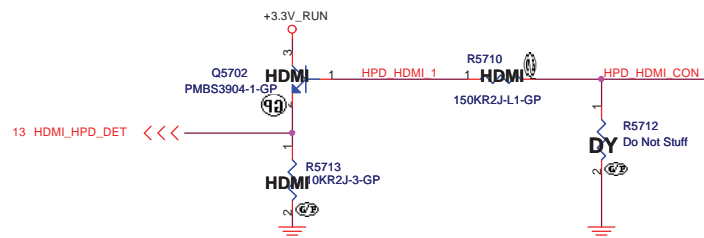
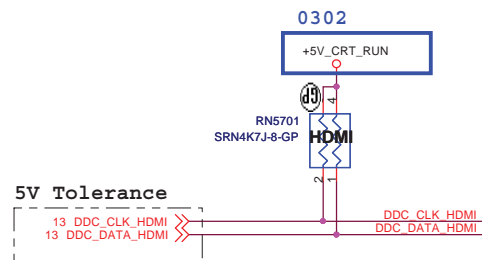
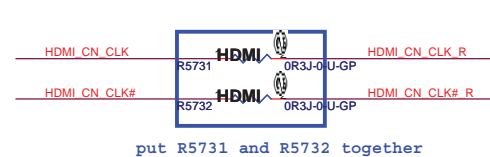
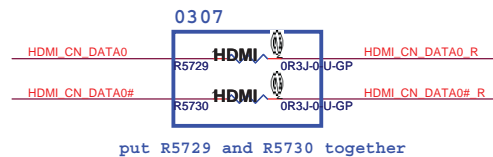
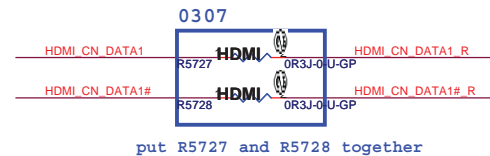
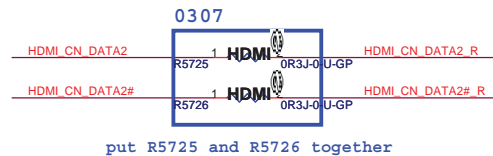
Reserved

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

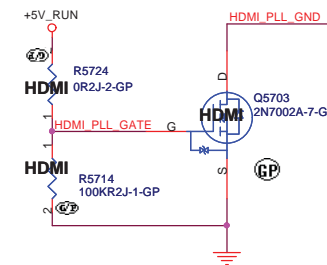
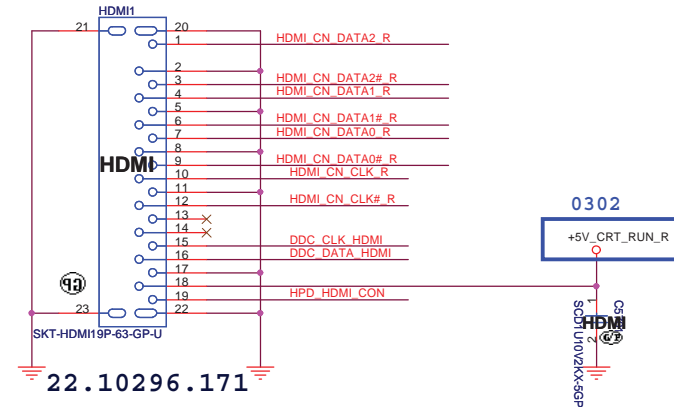
Date: Tuesday, April 13, 2010	Sheet 56 of 90
-------------------------------	----------------

SSID = VIDEO

HDMI CONNECTOR



HDMI CONN



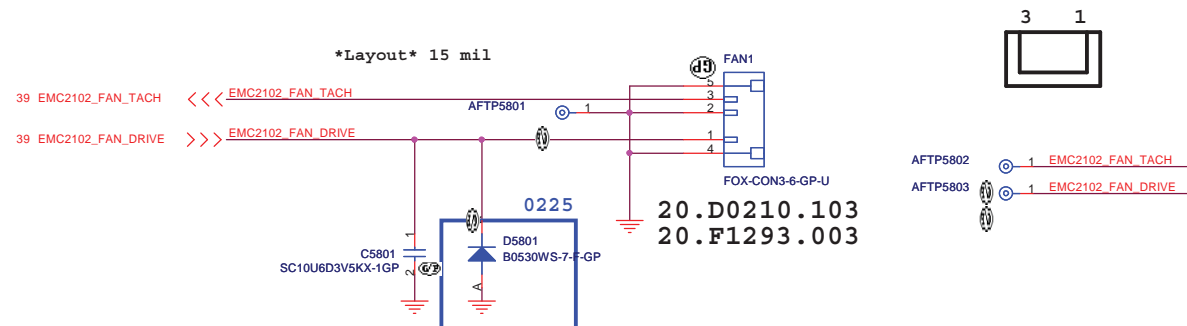
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

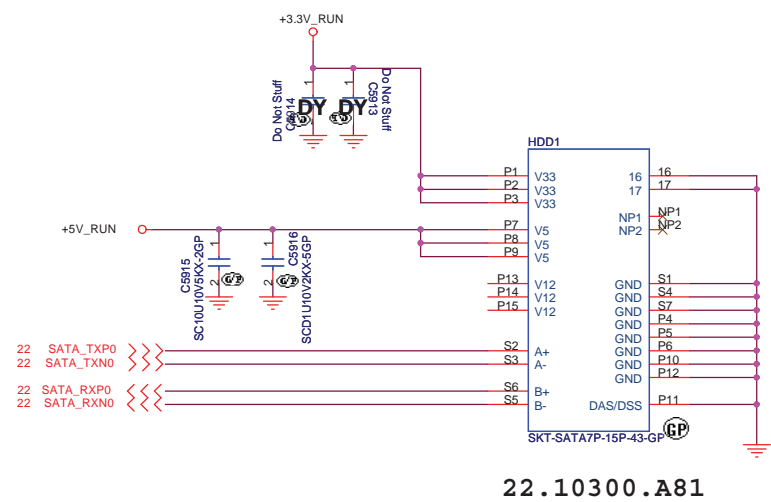
Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
Date:	Tuesday, April 13, 2010	Sheet 57 of 90

SSID = Thermal

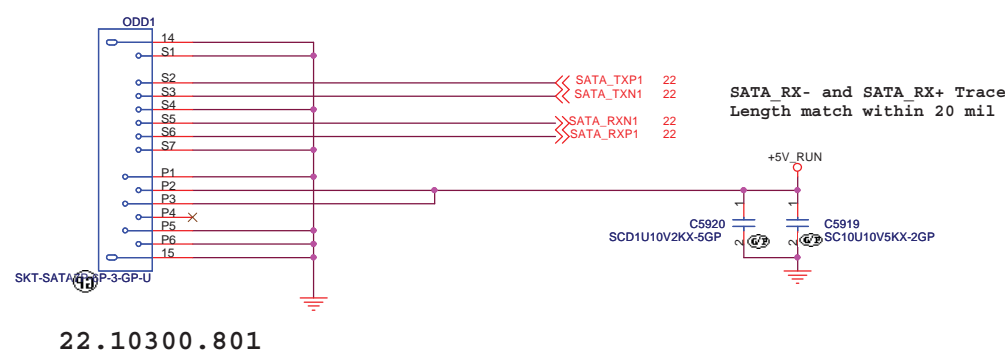
Fan Connector



SATA HDD Connector



ODD Connector

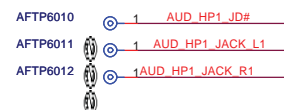
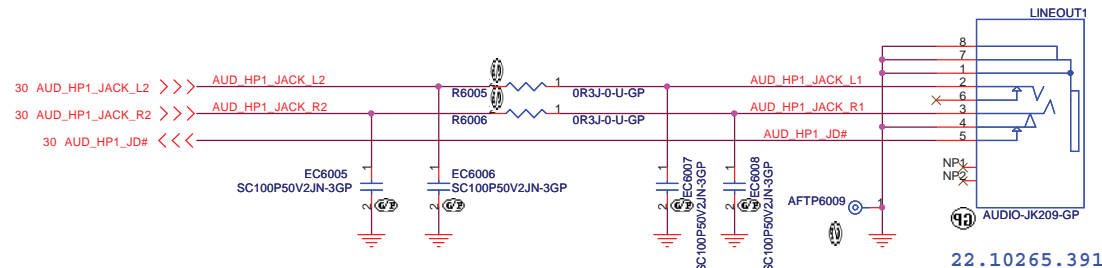
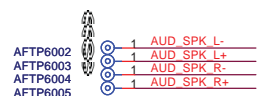
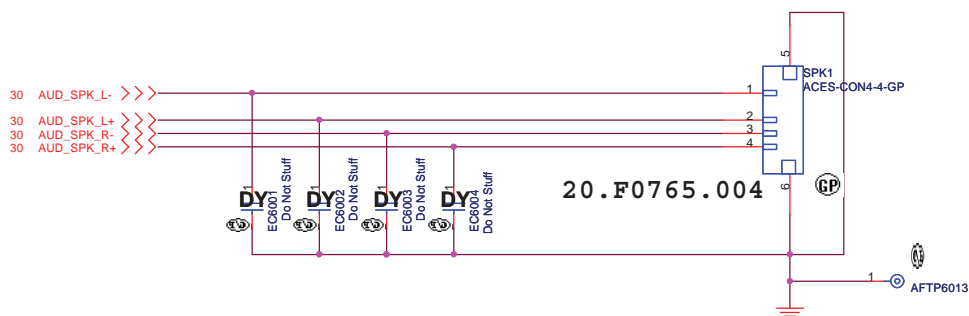


3 DJ2 AMD UMA (10 100 w HDMI)

SSID = AUDIO

Speaker Connector

LINE1 OUT

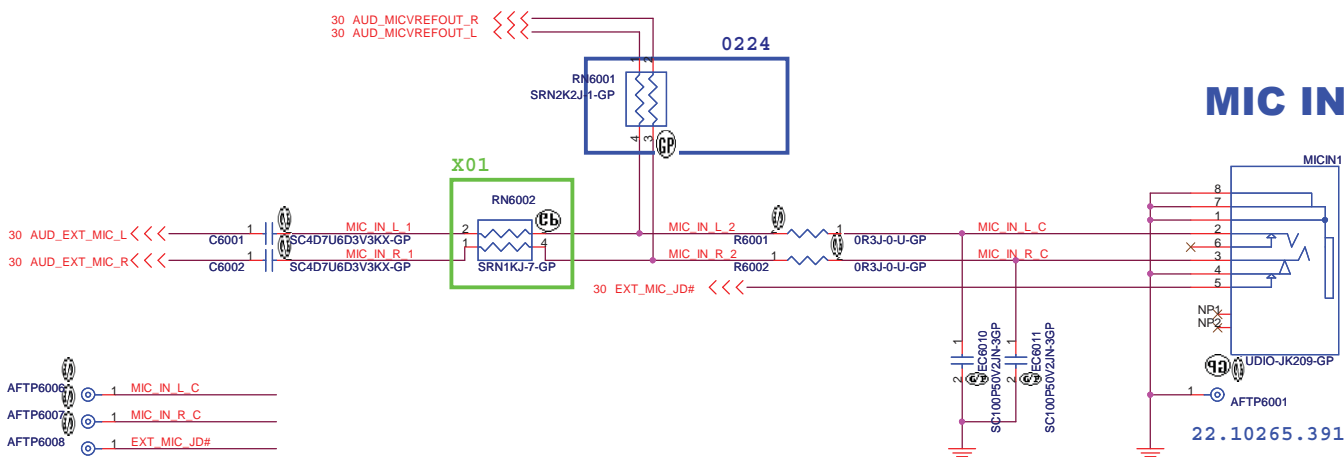


Internal Microphone

MIC1 is in DIP

MIC1 Do Not Stuff

23.42143.001



3 DJ2 AMD UMA (10 100 w HDMI)

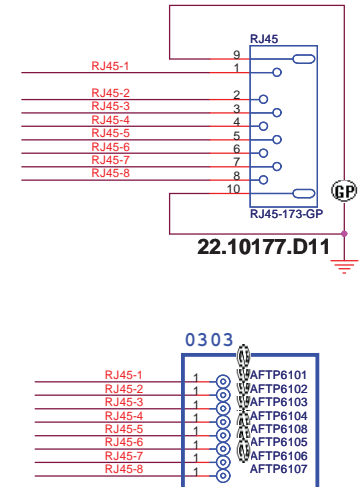


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

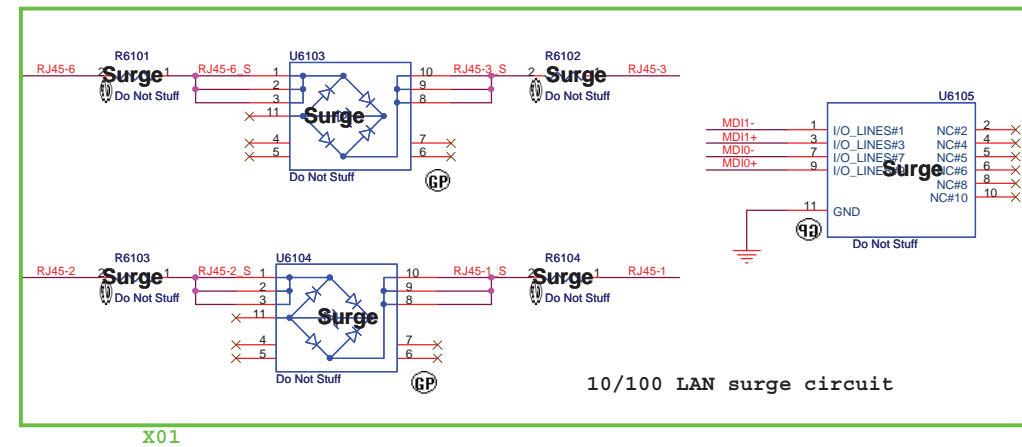
Title			Audio Jack	
Size	Document Number	Rev		
A3	Chelsea DJ2 AMD UMA	X01		
Date:	Tuesday, April 13, 2010	Sheet	60	of 90

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



Need to confirm use which XFORM for GIGA LAN
20100204



10/100 LAN surge circuit

DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

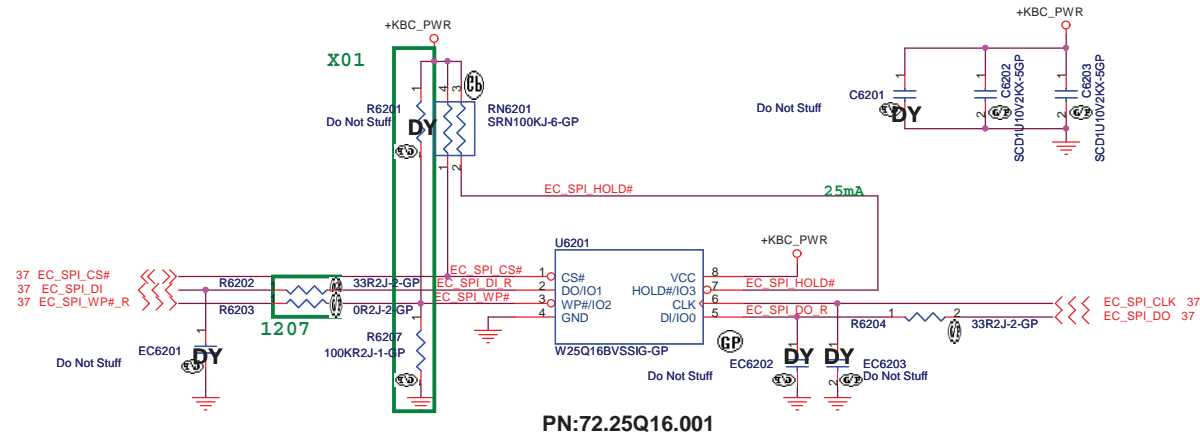
XFORM/RJ45

Chelsea DJ2 AMD UMA

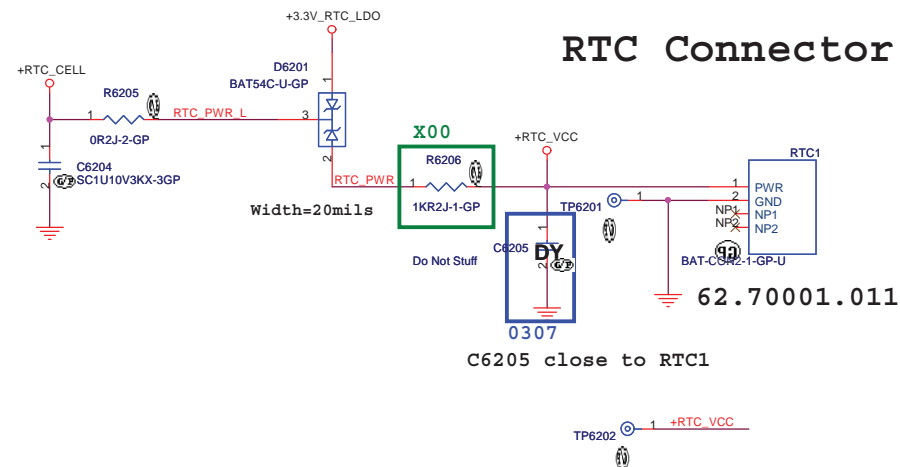
Sheet 61 of 90

SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



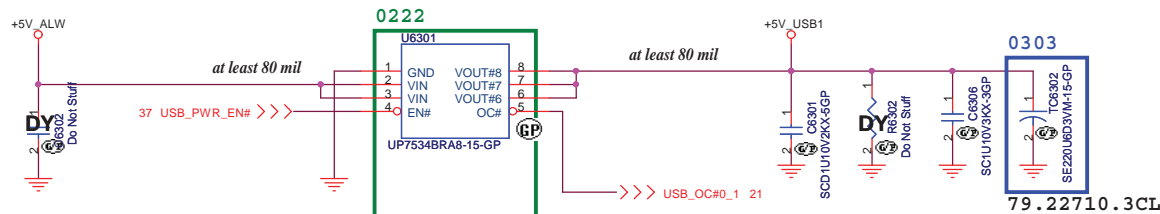
SSID = RBATT



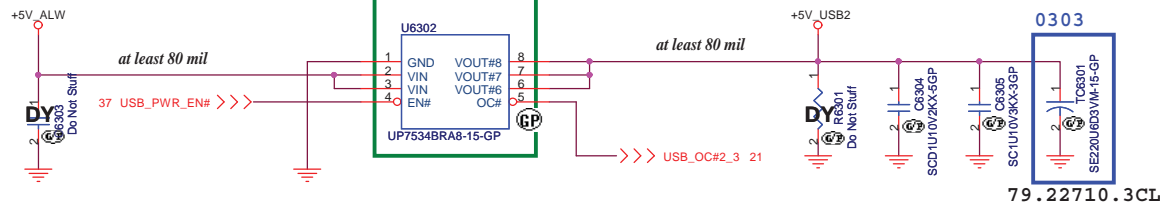
3 DJ2 AMD UMA (10 100 w HDMI)

SSID = USB

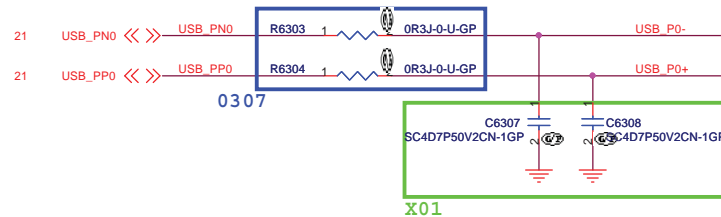
USB Power



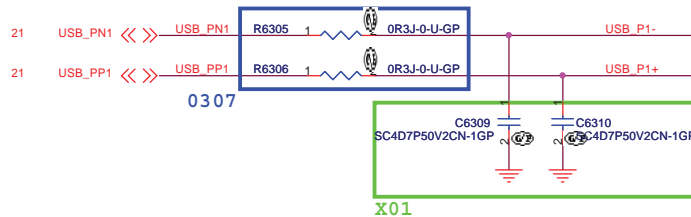
Right USB Power



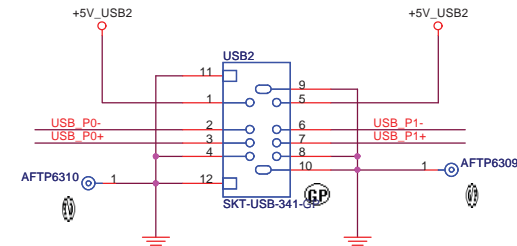
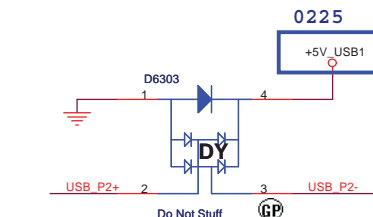
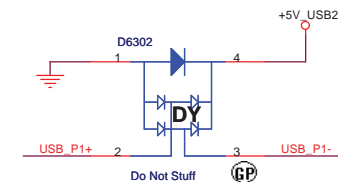
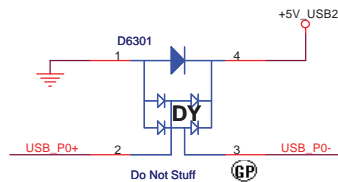
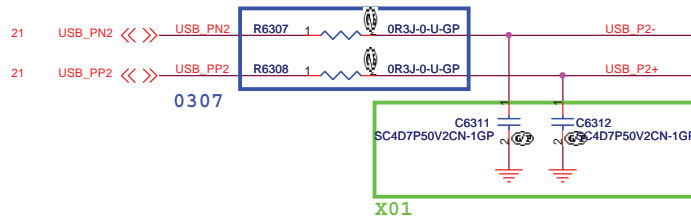
R6303,R6304 put together



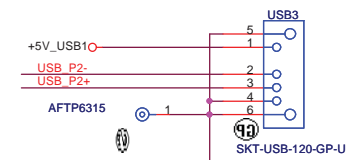
R6305,R6306 put together



R6307,R6308 put together



22.10254.501



22.10218.K71

AFTP6311	1	+5V_USB1
AFTP6304	1	+5V_USB2
AFTP6302	1	USB_P0-
AFTP6301	1	USB_P0+
AFTP6306	1	USB_P1-
AFTP6305	1	USB_P1+
AFTP6313	1	USB_P2-
AFTP6312	1	USB_P2+

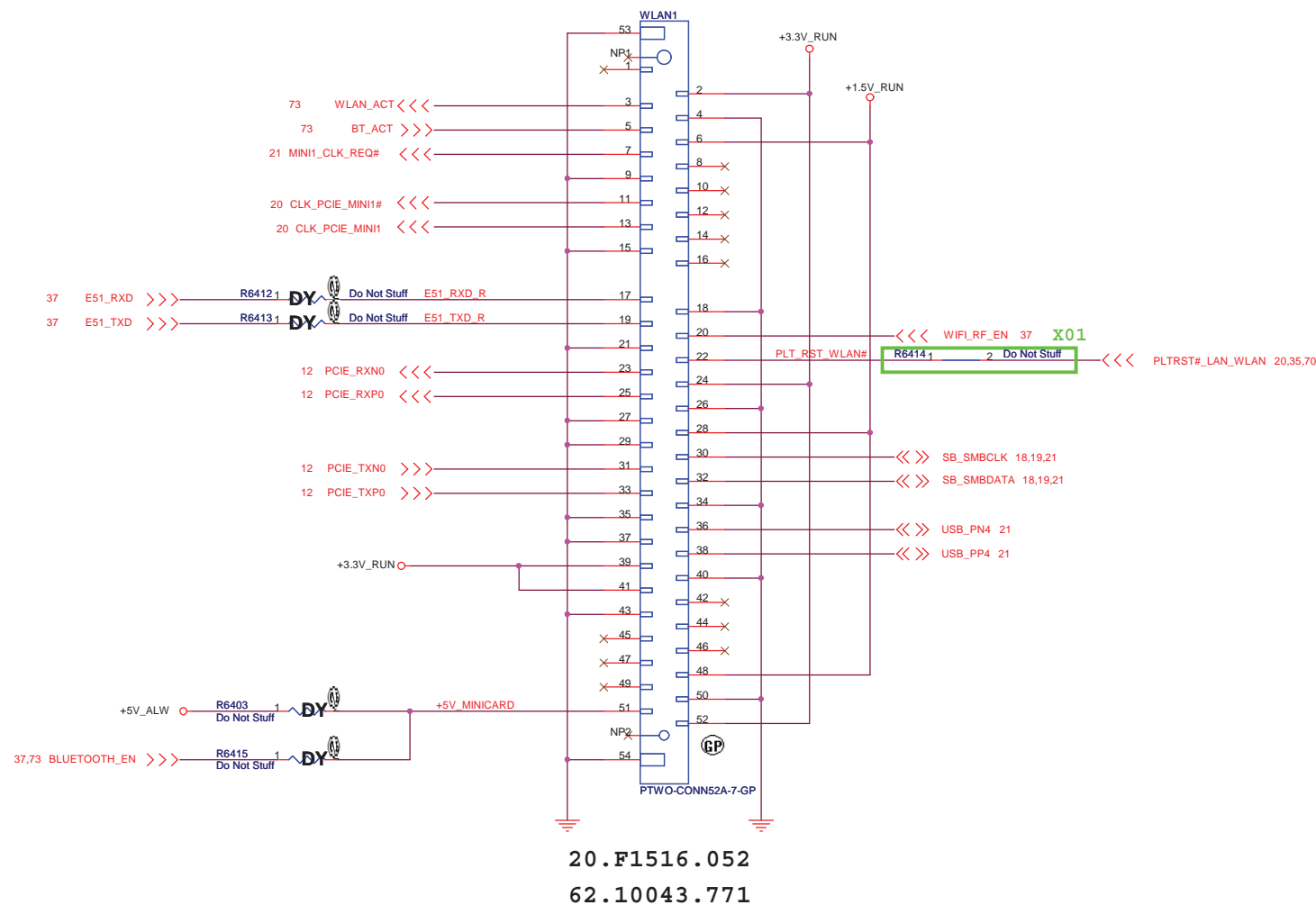
3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			USB		
Size	Document Number				Rev
	Chelsea DJ2 AMD UMA				X01
Date:	Wednesday, April 14, 2010				
	Sheet	63	of	90	


SSID = Wireless

Mini Card Connector(802.11a/b/g)



(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA

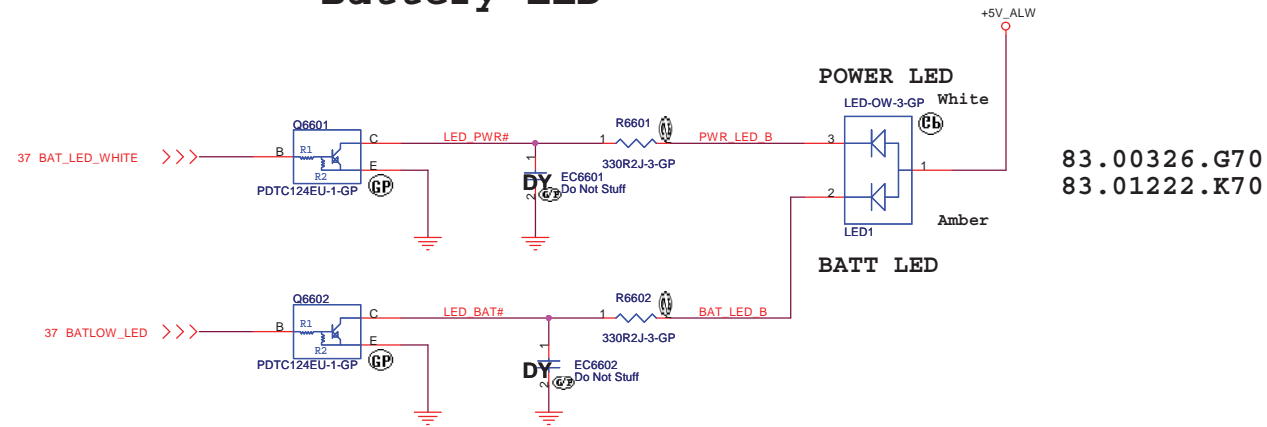
Rev
X01

Date: Tuesday, April 13, 2010

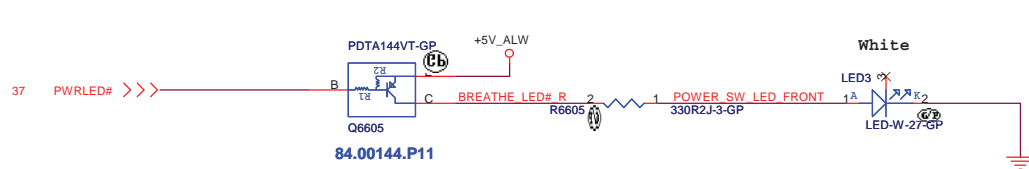
Sheet 65 of 90

SSID = User.Interface

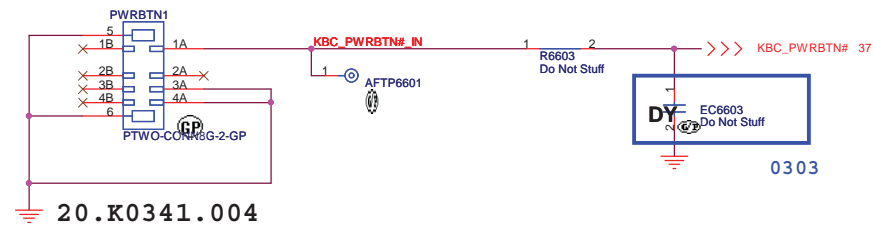
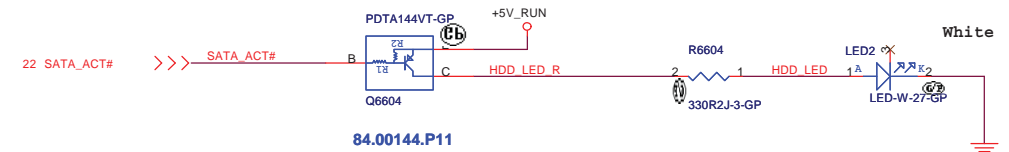
Battery LED



BREATHE PWR LED (Front)



HDD LED




3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			LED/PWRBTN	
Size	Document Number	Rev		
A3	Chelsea DJ2 AMD UMA	X01		
Date:	Tuesday, April 13, 2010	Sheet	66	of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

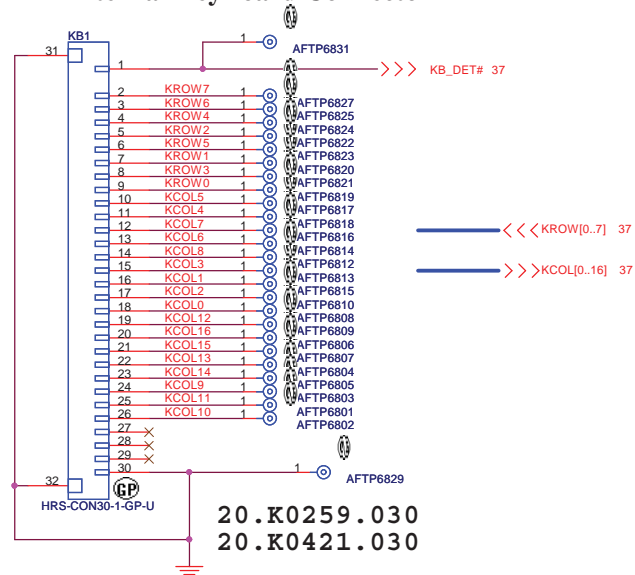
Document Number
Chelsea DJ2 AMD UMA

Rev
X01

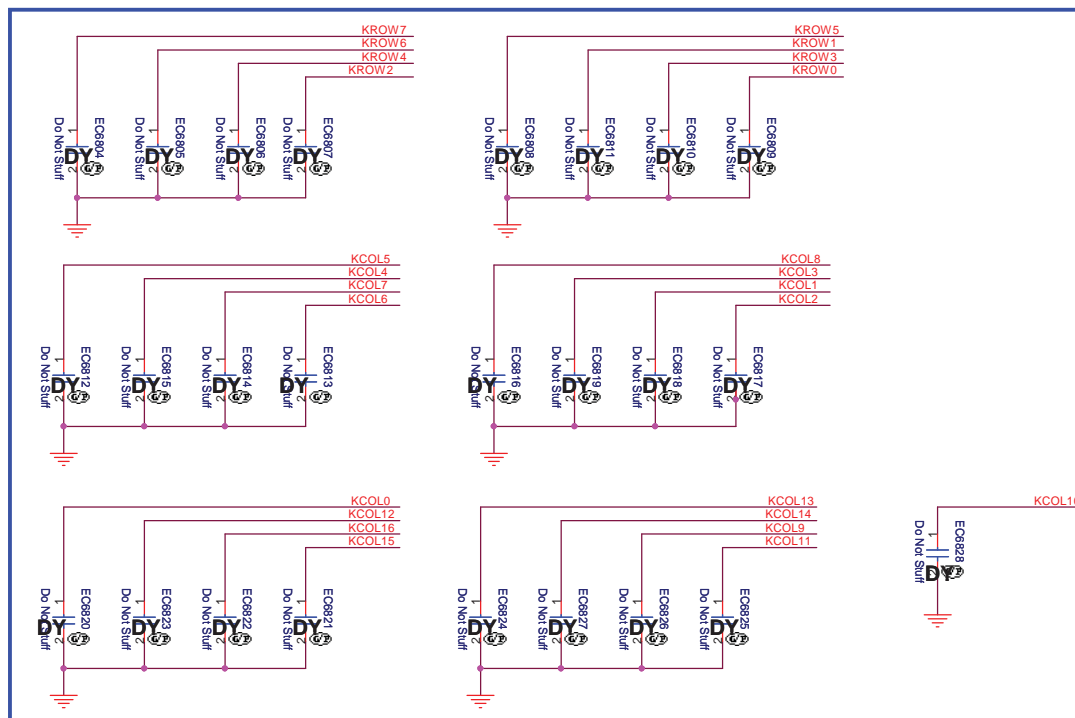
Date: Tuesday, April 13, 2010Sheet 67 of 90

SSID = KBC

Internal Keyboard Connector

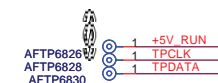
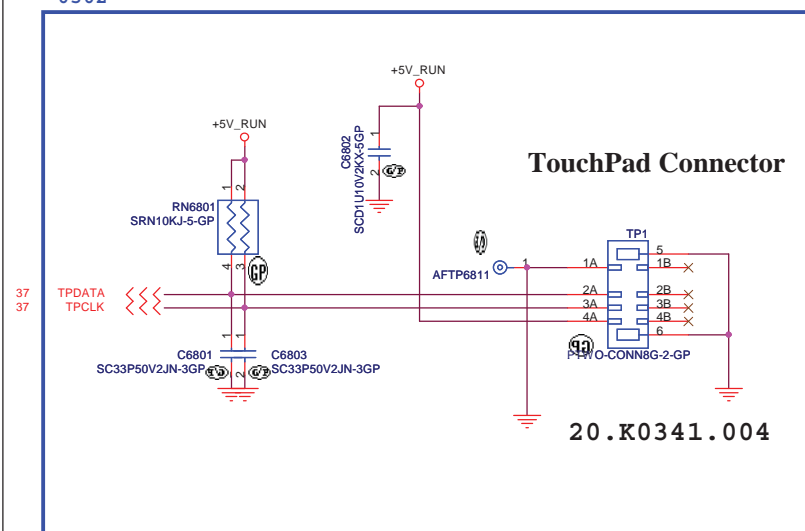


0304



SSID = Touch.Pad

0302



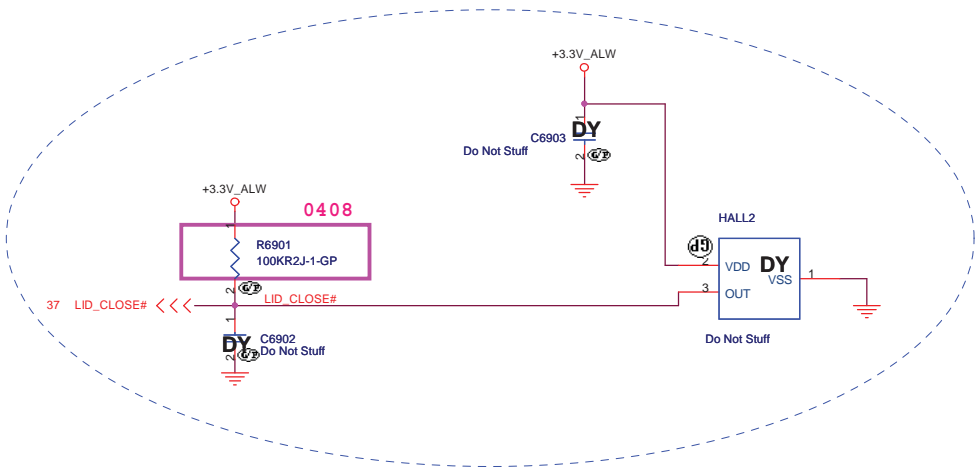
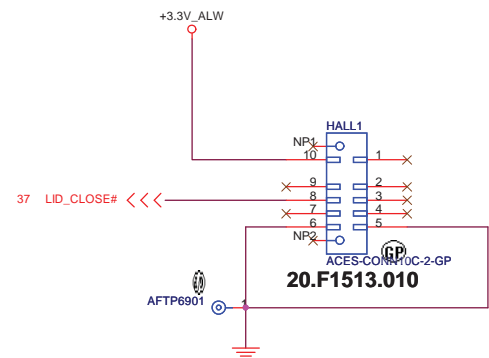
3 DJ2 AMD UMA (10 100 w HDMI)

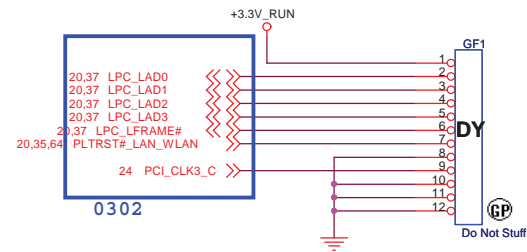


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Key Board/Touch Pad		
Size	Document Number	Rev
A3	Chelsea DJ2 AMD UMA	X01
Date:	Tuesday, April 13, 2010	Sheet 68 of 90

SSID = User. Interface



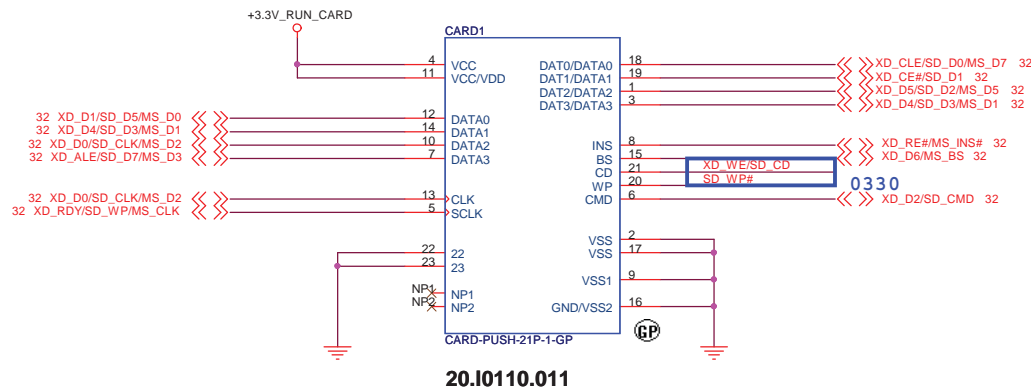
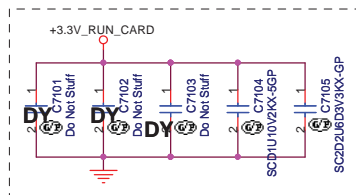


3 DJ2 AMD UMA (10 100 w HDMI)

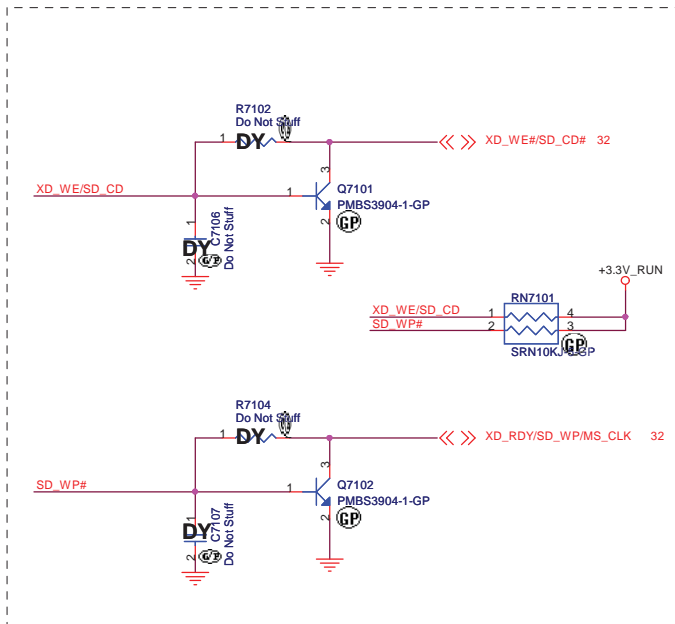
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Chelsea DJ2 AMD UMA		Rev X01
Date: Tuesday, April 13, 2010	Sheet 70	of 90	

SSID = SDIO

SD/XD/MS Card Reader



For reverse card connector 0330




3 DJ2 AMD UMA (10 100 w HDMI)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CARD Reader Connector		
Size			Document Number		
A3			Chelsea DJ2 AMD UMA		
Date: Tuesday, April 13, 2010			Rev X01		
Sheet 71			of 90		

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A3

Document Number
Chelsea DJ2 AMD UMA

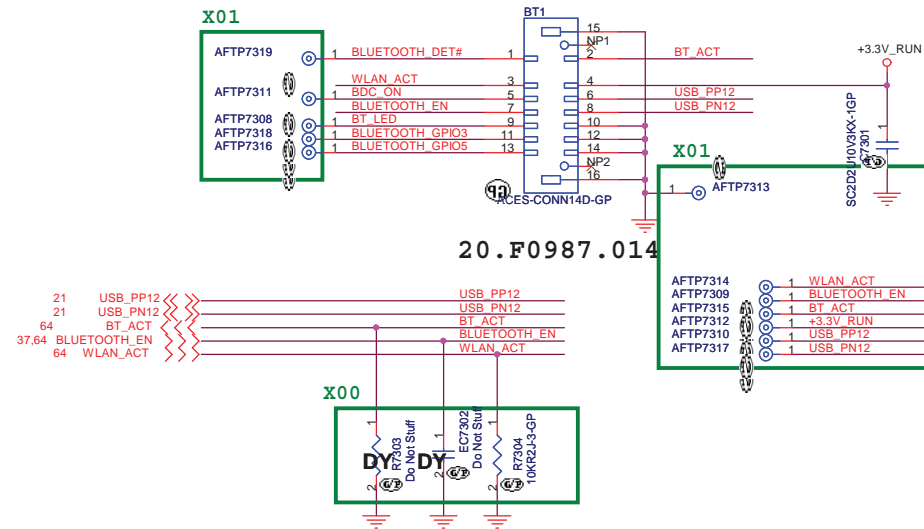
Rev
X01

Date: Tuesday, April 13, 2010

Sheet 72 of 90

SSID = User.Interface

Bluetooth Module conn.



3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Bluetooth

Size
A3

Document Number

Chelsea DJ2 AMD UMA

Rev


X01

Date: Tuesday, April 13, 2010

Sheet 73 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

Date: Tuesday, April 13, 2010	Sheet 74 of 90
-------------------------------	----------------

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Rev
X01

Date: Tuesday, April 13, 2010

Sheet 75 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


IO Board Connector

Size A3	Document Number Chelsea DJ2 AMD UMA	Rev X01
------------	---	-------------------

Date: Tuesday, April 13, 2010	Sheet 76 of 90
-------------------------------	----------------

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Rev
X01

Date: Tuesday, April 13, 2010

Sheet 77 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

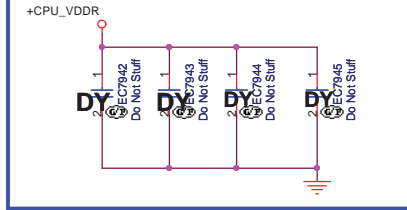
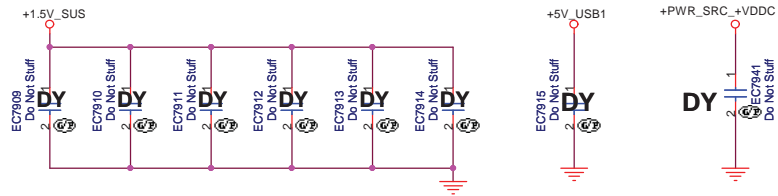
Document Number
Chelsea DJ2 AMD UMA

Date: Tuesday, April 13, 2010

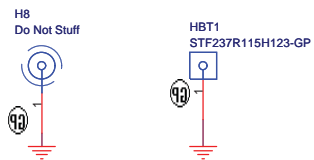
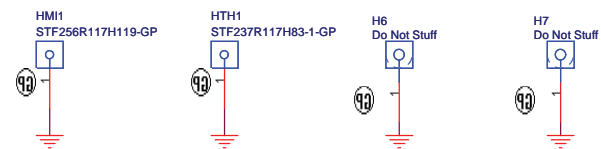
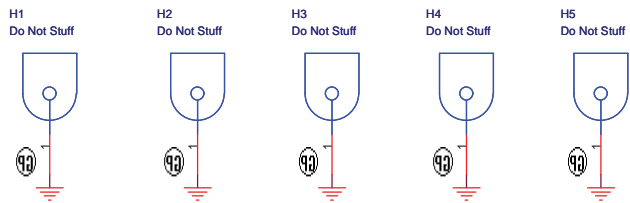
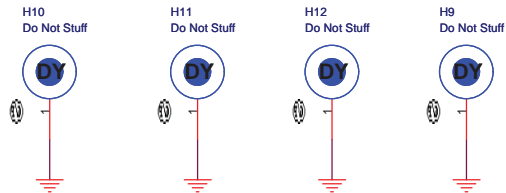
Rev
X01

Sheet 78 of 90

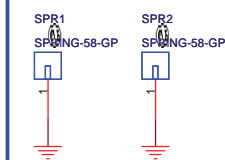
EMI Request



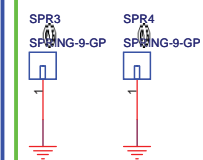
0307



0311



X01



3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
UNUSED PARTS/EMI Capacitors			
Size	Document Number		Rev
A3	Chelsea DJ2 AMD UMA		X01
Date:	Tuesday, April 13, 2010	Sheet 79 of 90	

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VGA PCIE(1/4)

Size

A3

Document Number

Chelsea DJ2 AMD UMA

Rev


X01

Date: Tuesday, April 13, 2010

Sheet 80 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VGA LVDS/TV/CRT(2/4)

Size

A3

Document Number

Chelsea DJ2 AMD UMA

Rev


X01

Date: Tuesday, April 13, 2010

Sheet 81 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VGA POWER/GND(3/4)

Size

Document Number

Rev

A3

Chelsea DJ2 AMD UMA


X01

Date: Tuesday, April 13, 2010

Sheet 82 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

A3

Chelsea DJ2 AMD UMA


X01

Date: Tuesday, April 13, 2010

Sheet 83 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM (1/2)

Size

Document Number

Rev

A3

Chelsea DJ2 AMD UMA

X01


Date: Tuesday, April 13, 2010

Sheet 84 of 90

1

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM (2/2)

Size
A3

Document Number
Chelsea DJ2 AMD UMA

Rev
X01

Date: Tuesday, April 13, 2010

Sheet 85 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TPS51117 +VCC GFXCORE

Size
A3

Document Number
Chelsea DJ2 AMD UMA

Rev
X01

Date: Tuesday, April 13, 2010

Sheet 86 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

APL5930 +1.1V RUN

Size
A3

Document Number
Chelsea DJ2 AMD UMA


Rev
X01

Date: Tuesday, April 13, 2010

Sheet 87 of 90

(Blanking)

3 DJ2 AMD UMA (10 100 w HDMI)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A3

Document Number

Chelsea DJ2 AMD UMA

Rev

X01

Date: Tuesday, April 13, 2010

Sheet 88 of 90

[illegible]

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.